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PROPERTIES OF TWO DIODE FREQUENCY DOUBLERS

by

© WILFRED JOHN CAMERON

A THESIS
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The undersigned certify that they have read, and recommend to the Faculty of Graduate Studies for acceptance, a thesis entitled "Properties of Two Diode Frequency Multipliers" submitted by W.J. Cameron in partial fulfilment of the requirements for the degree of Master of Science.

ABSTRACT

Step recovery diodes (S.R.D.'s) are now developed to the extent that appreciable power can be supplied at U.H.F. and microwave frequencies by solid state, S.R.D. harmonic generators. However, if a single diode has insufficient power handling capability for a particular application, one or a combination of the following techniques is often utilized;

(1) Replace the single diode by an N-diode array or chain, thus increasing the power handling capability by N.

(2) Combine the outputs of N separate harmonic generators by means of a summing device.

This thesis deals with a practical design technique of the 2nd type (summing) for a two diode frequency doubler. The object is to demonstrate that comparable performance and circuit symplicity can be achieved utilizing the summing technique.

Initially the one diode doubler is analyzed and experimental results for two such multipliers are given. From the data obtained a method is proposed which would provide for greater ease in tuning a multiplier containing several stages.

Following this, the design and performance of two frequency doublers, each employing two diodes, are given. The first uses the $\lambda/2$ phase shift array principle as described by Parker and Grayzel in 1966. The second consists of two separate doublers, with a device to sum their outputs. The summing device, a stripline adaptation of the Wilkinson hybrid circuit, provided the necessary isolation between output ports and had low insertion loss.

ACKNOWLEDGEMENT

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CHAPTER 1

Introduction

Harmonic frequency multipliers are normally two-port networks consisting of one or more non-linear devices in connection with wave filters. The input terminals accept an input power (P_{IN}) at a frequency F_{IN}, and the output (P_{out}) is available at an output frequency $F_{out}=nF_{IN}$, where n=2,3,4..... . Since the output frequency is an integral multiple of the input, the frequency stability of the output will be the same as that of the input. The efficiency, $\eta = P_{out}/P_{IN}$, depends on the driving frequency, order of multiplication, power level, and the non-linear device employed. Figure 1.1 illustrates the basic components of a harmonic generator.

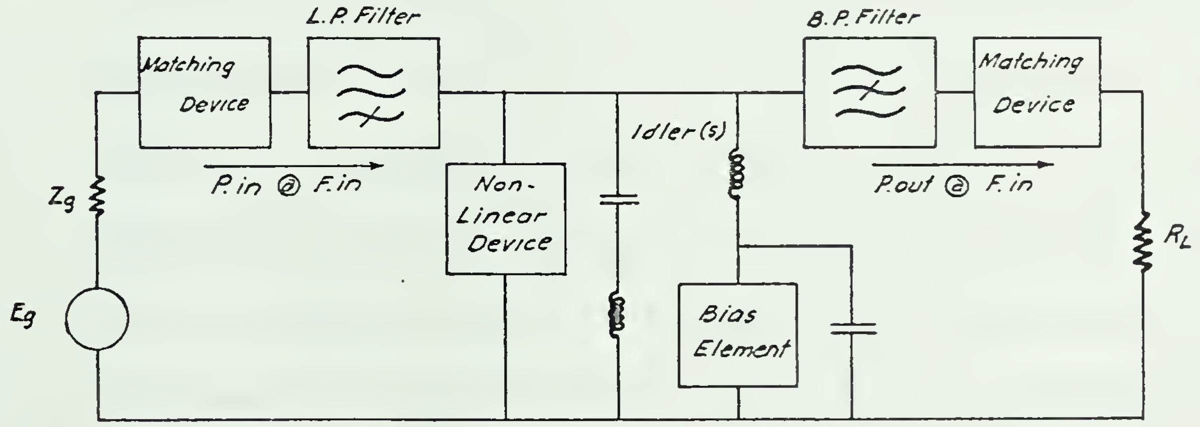


FIG. 1.1 HARMONIC GENERATOR

The basic electrical requirements of a single stage multiplier as shown in Fig. 1.1 are:

(A) The input must pass power at the driving frequency only. Harmonics generated in the device must be reactively isolated from the input circuit to prevent undesired power dissipation in the source impedance, and the disruption of the operation of the preceeding multiplier if one exists.

(B) For maximum conversion efficiency, the source and load must be conjugately matched to the device by suitable networks.

(C) Power must be allowed to flow in the output circuit at the output frequency only for reasons analogous to those given in (A).

(D) For multiplication ratios greater than two, currents at intermediate harmonics (less than the output frequency) may be allowed to flow through the non-linear device by the use of parallel connected, lossless, series-tuned "idler" circuits. Although not present at the input or output, these idler currents interact with the fundamental and various harmonics to give more efficient generation of the desired output.

(E) A suitable bias voltage across the device is necessary. This is usually accomplished in one of two ways: self bias using a resistor or fixed bias using an external power supply.

The non-linear capacitance and charge storage characteristics of the varactor (variable reactance) diode make it an ideal device for frequency multiplication.

It has gained popularity in applications where reliable solid state microwave power is required, such as local oscillators, parametric amplifier pumps and transmitters. Varactors are semiconductor P-N junction diodes which exhibit a useful, voltage-dependent capacitance when they are biased between the forward conduction region and reverse breakdown. Most are made from silicon, gallium arsenide or germanium, their characteristics optimized by the proper choice of semiconductor material and fabrication technique. In reverse bias, the capacitance as a function of voltage can be expressed by the following equation (Fig. 1.2),

$$C_T = C_P + \frac{C_{jo}}{\left(1 + \frac{V_B}{\phi}\right)^n} \quad \ldots\ldots\ldots\ldots\ldots\ldots (1.1)$$

where C_T = total capacitance of varactor

C_P = package capacitance

C_{jo} = junction capacitance at zero bias

V_B = applied reverse bias

ϕ = contact potential

$\underline{n}$ = exponent of capacitance variation*

---

* The exponent $\underline{n}$ is a function of the junction type (ie) $\underline{n} = \frac{1}{2}$ for abrupt (alloyed) junction, $\underline{n} = 1/3$ for graded (diffussed) junction.

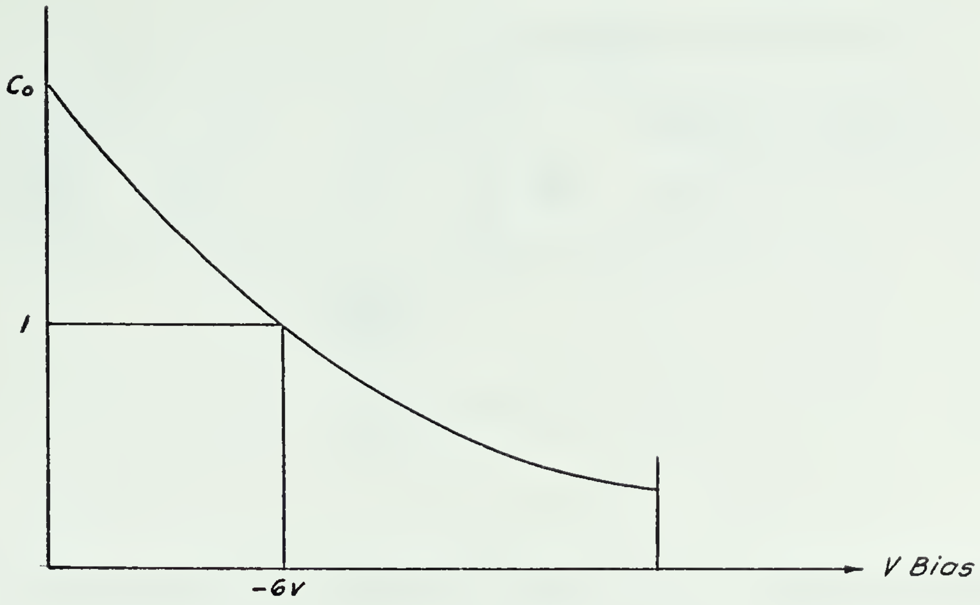


FIG. 1.2 NORMALIZED JUNCTION CAPACITANCE OF A TYPICAL VARACTOR

This relationship can be predicted from the depletion layer behavior. Under reverse bias, the structure acts very much like a charged capacitor, with the depletion layer representing the dielectric and the semiconductor material adjacent to the depletion layer representing the two conductive plates (FIG. 1.3). If an external voltage is applied across the junction as to reinforce the contact potential (reverse bias), the depletion layer width increases resulting in a capacitive decrease. If a forward voltage is applied, the depletion layer width decreases. However, if the external voltage is sufficiently large so that the device is driven near or to forward conduction, two correction capacitances become important. The first accounts for the fact that the depletion layer is not well defined because of imperfect shielding of majority carriers, and the other accounts for charge stored in the injected minority carriers (diffusion capacitance).

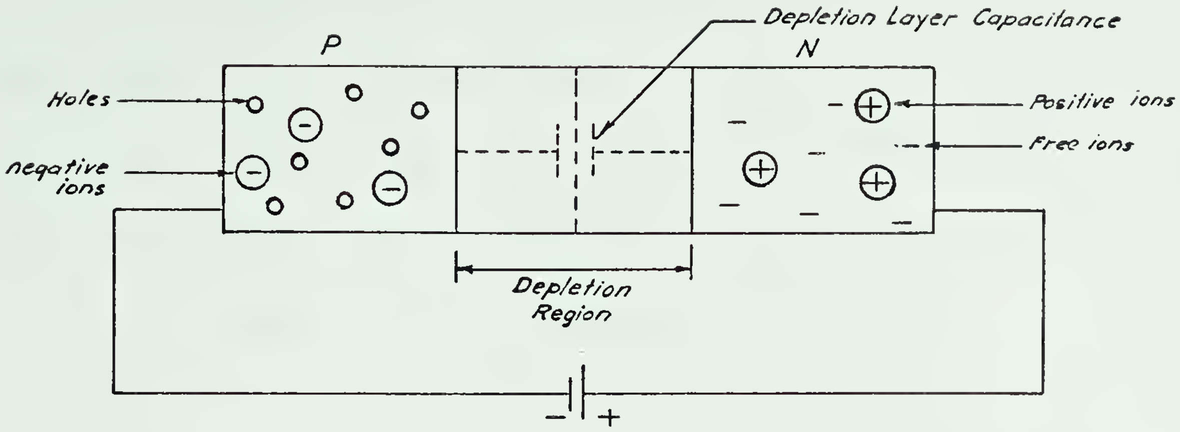


FIG. 1.3 P-N Junction (Simplified) Under Reverse Bias

When fully driven or over driven (forward conduction occuring) all three mechanisms contribute to harmonic generation, their relative importance being dependent on the doping profile. For $\underline{n} = \frac{1}{2}$ and 1/3 (step and linearily graded junction), variation of depletion layer capacitance in the reverse bias region is the principal cause of non-linearity. For $\underline{n} \approx .2$, a typical range for the step recovery varactor, charge storage is the predominant effect. This diode type has gained wide popularity for its greater power handling capability and linearity of power output with changes in input power.

The relationship between power handling capability (P_r) and varactor characteristics is given by:

$$P_r \propto C_o V_B^2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1.2)$$

where V_B = voltage (reverse bias) breakdown of the junction

C_o = junction capacity at zero bias.

When a single diode has insufficient power handling capability for a desired application, n diodes

are often combined such that they are electrically equivalent to a single diode having approximately n times the power handling capability. This equivalence must be achieved at the input, output and idling frequencies. As a simple example, placing two varactors in series, where their physical dimensions were much less than a quarter wavelength, would effectively double the power handling capability. A second method for obtaining high output power would be the summation of power from n separate multipliers. Although seemingly less complicated from a design viewpoint, a major disadvantage would seem to be cost as n circuits of the type shown in Figure 1.1, and a summing device would be necessary. However, with proper isolation between multipliers, the problem of instability in the form of "chain" oscillation due to higher order resonances (which may be unknowingly introduced in a conventional varactor array) would be greatly reduced.

The purpose of this study is to examine and verify a practical design technique for a high power, two-diode, frequency doubler. Background material in Chapter two concerning the step recovery diode operation, the one diode multiplier and present techniques of combining diodes in multi-diode multipliers, is presented for purposes of comparison and understanding of the ensuing chapters. In order to give greater insight into practical design methods of frequency multipliers and step recovery

diode phenomena, the one-diode doubler was initially considered. The design and performance of two such multipliers with a proposed method of tuning an n varactor chain is given in Chapter three. This is followed by a study of higher power multipliers in Chapter four. Initially the theoretical performance and experimental results for the $\lambda/2$, two diode doubler constructed are discussed as the $\lambda/2$ phase shift array is perhaps the most common method utilized for combining diodes in high power multipliers.

The latter part of the chapter deals with the design and performance of the stripline adaptation of the Wilkinson power divider (used as a summing device) and the circuit (addition of power from two separate multipliers) in which it is employed. A comparison is made between this multiplier and those designed using conventional methods. Conclusions are given in Chapter five.

CHAPTER II

Review Of Step Recovery Diode And Frequency Multiplier Theory

2.1 Qualitative Analysis Of The Step Recovery Diode

Step recovery in P-N junctions(1,2,3,4) is a function of charge storage, a familiar phenomenon in the application of semiconductor devices. With a P-N junction forward biased, majority carriers from one region (P or N) are injected into the other (N or P) to form minority carriers. If permitted to remain there for a sufficient amount of time, these minority carriers recombine with majority carriers to produce current flow. The time interval between injection and recombination is related to the minority carrier lifetime of the material. In the interval between the time of injection and recombination, these minority carriers are effectively stored charges contributing to junction capacitance.

If the time interval when the junction is forward biased is less than the carrier lifetime, a majority of the injected carriers can be swept back across the junction to become majority carriers again before significant recombination occurs. Step recovery occurs when the minority carriers are returned in a bunch. Such a movement of carriers constitutes a current waveform as shown in Fig. 2.1.

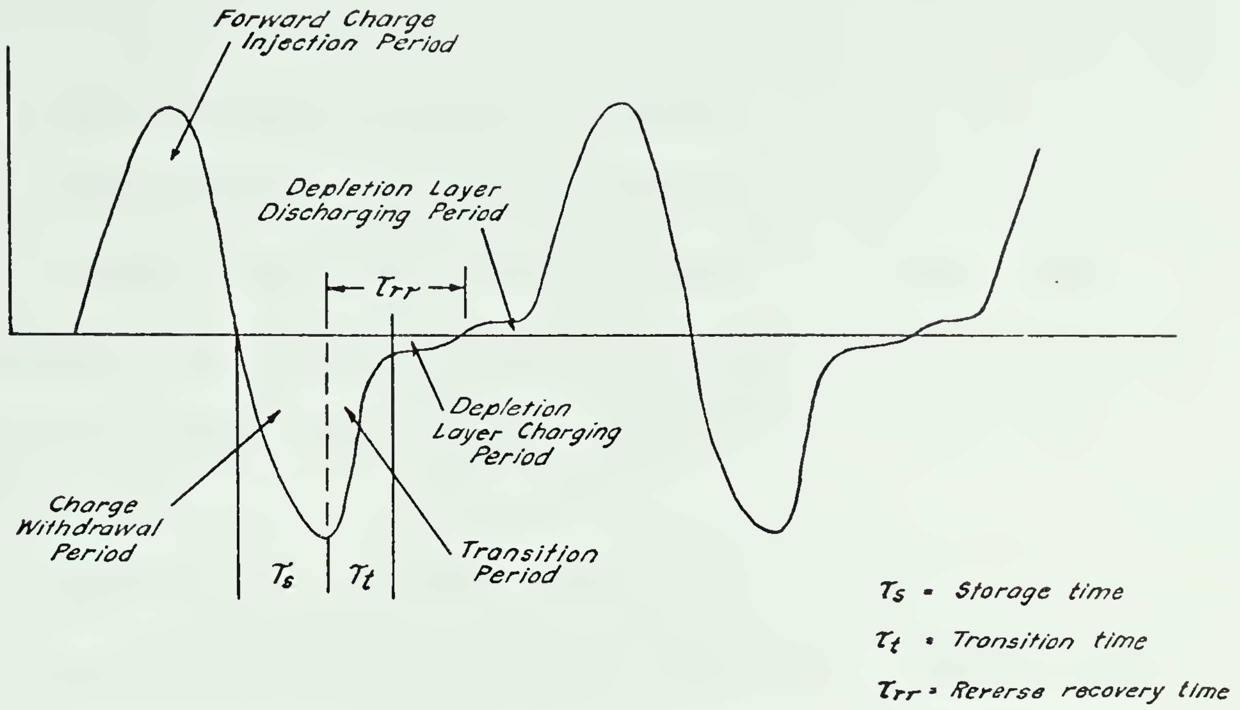


FIG. 2.1 MICROWAVE CURRENT WAVEFORM OF SINUSOIDALLY SWITCHED STEP RECOVERY DIODE

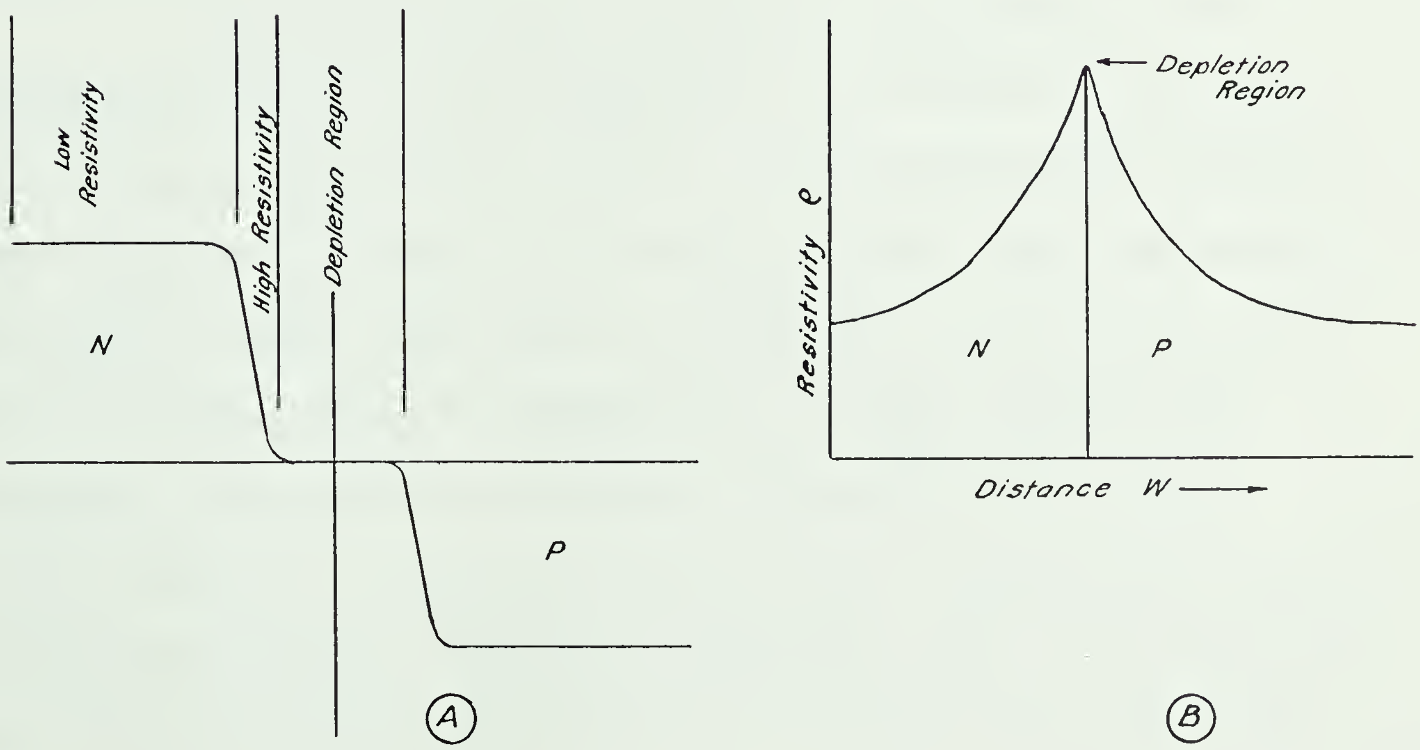


FIG. 2.2 IMPURITY PROFILE OF STEP RECOVERY DIODE

The impurity profile(5) shown in Fig. 2.2 enchances step recovery as the electric fields set up by the steep impurity gradient, only a short distance away from the depletion region, tend to confine the minority carriers to the depletion layer, rather than permitting them to disperse.

Application of the step recovery mechanism yields a frequency multiplier with relatively linear power characteristics since the percentage of harmonic current generation is not a significant function of signal level. If self-biasing is employed, the shape of the current wave remains constant over a considerable input power range.

Series resistance, which is the primary loss mechanism common to all varactors, is a function of voltage in the step recovery diode. By employing the impurity profile shown in Fig. 2.2, the resistivity near the junction can be made high (thus, increasing reverse bias breakdown voltage) without changing the average resistivity. Moreover, when reverse voltage is applied, the spread of the depletion region (∞ resistivity) into the high resistivity regions actually dissipates them, leaving only the low resistivity portion of the material to contribute

to r_s. As the time the varactor is in the reverse bias condition is large compared to the forward-bias condition, the total series resistance, (thus loss) is substantially reduced despite the increase in resistivity at the junction.

2.2 Mathematical Model For The One-Diode Doubler(6,7,8)

To simplify the following analysis, it is assumed that the minority carrier lifetime is infinite and that the diode has an ideal step function capacitance voltage relationship in which C_{MAX} is very large so that $S_{MIN} = 1/C_{MAX} \rightarrow 0$ (Fig. 2.3). The schematic diagram of the multiplier considered is shown in Fig. 2.4. Since the multiplier considered here contains no idlers, only currents i_o and i_n are allowed to flow. (Fig. 2.4).

Let the charge waveform be given by:

$$q = q_o \sin(w_o t + \theta_o) + q_n \sin(w_n t + \theta_n) \text{ ....} (2.1)$$

where $w_n = nw_o$. Then the current is given by:

$$i = \frac{dq}{dt} = q_o w_o \cos(w_o t + \theta_o) + w_n q_n \cos(w_n t + \theta_n) \text{.....} (2.2)$$

Assuming that q = o at t = o and that n is even, the elastance waveform will be a square waveform function of time given by:

$$S(t) = \frac{S_{MAX}}{2} \left[1 + \sum_{K=1}^{\infty} \frac{4}{\pi} \left\{ \frac{1-(-1)^K}{2K} \right\} \sin K w_o t \right] \text{....} (2.3)$$

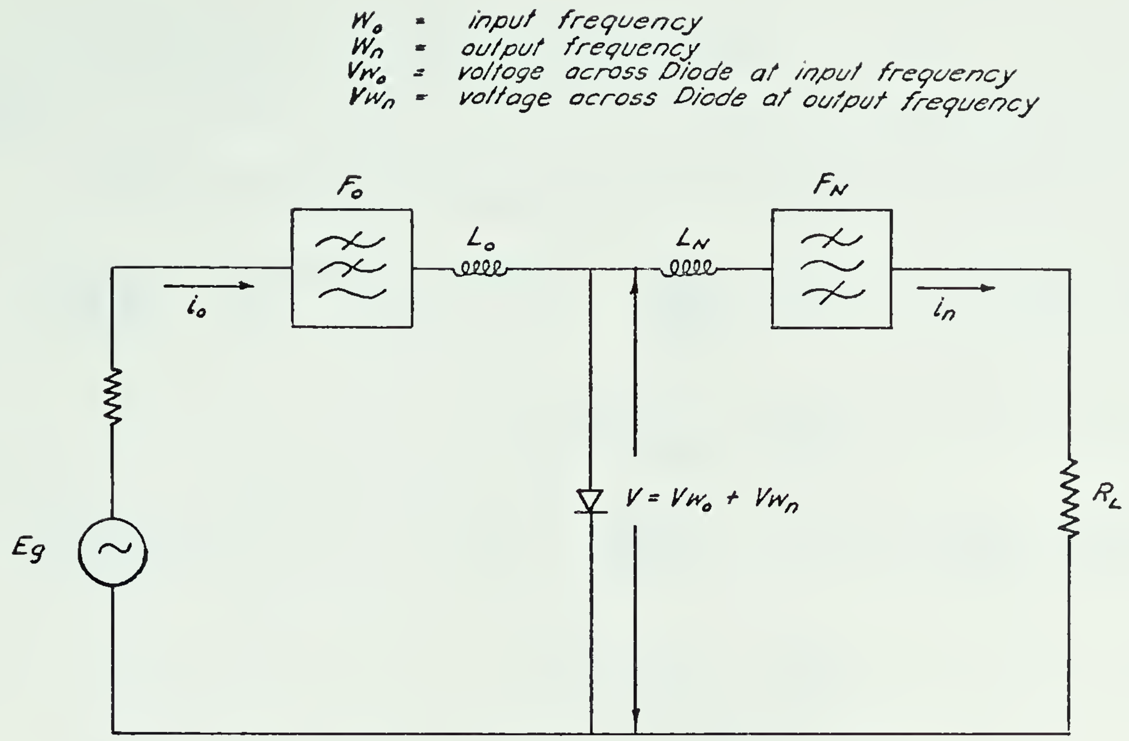


FIG. 2.4 Schematic Diagram Of Multiplier

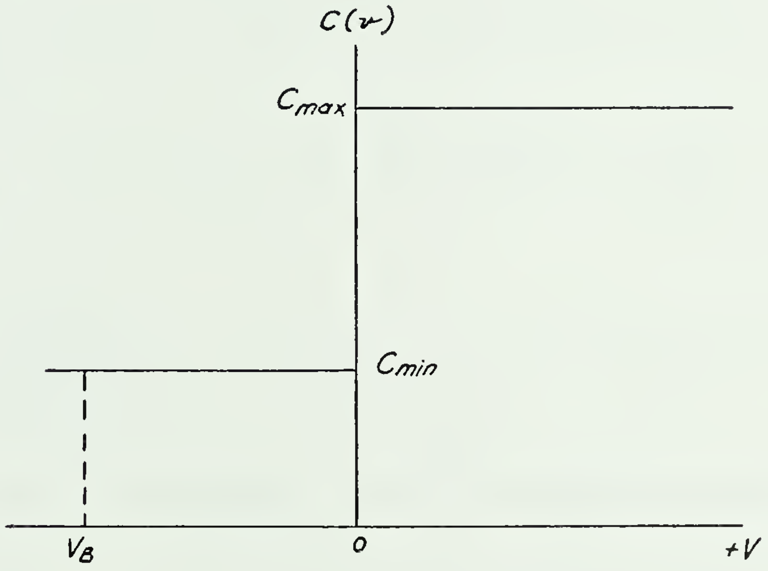


FIG. 2.3 Idealized Capacitance Vs. Voltage

The diode voltage is given by:

$$V(t) = \int S(t).i(t)dt \qquad \ldots\ldots(2.4)$$

Substitution of equations 2.2 and 2.3 into 2.4 yields

$$V_{w_o}(t) = \frac{S_{MAX}}{2} q_o \sin(w_o t + \theta_o) - \frac{S_{MAX}}{w_o} q_n w_n \frac{\cos(w_o t - \theta_n)}{n + 1} - \frac{\cos(w_o t + \theta_n)}{n - 1} \qquad \ldots\ldots(2.5)$$

$$V_{w_n}(t) = \frac{S_{MAX}}{2} q_n \sin(w_n t + \theta_n) - \frac{S_{MAX}}{n} q_o w_o \frac{\cos(w_n t + \theta_o)}{n - 1} + \frac{\cos(w_o t - \theta_n)}{n + 1} \qquad \ldots\ldots(2.6)$$

Hence the input power is given by:

$$P(w_o) = \frac{w_o}{2} \int_o^{2\pi/w_o} V_{w_o}(t) \,.\, (q_o w_o \cos(w_o t + \theta_o)dt \qquad \ldots\ldots(2.7)$$

If $\theta_o = o$, the maximum value of $P(w_o)$ occurs when $\theta_n =$ $(2S + 1)$ where S is an integer, ie.

$$P(w_o)_{MAX} = \frac{w_n S_{MAX}}{\pi\,(n^2-1)} q_o q_n \qquad \ldots\ldots(2.8)$$

If the conversion efficiency of the diode is η, the output power is given by:

$$P(w_n)_{MAX} = \frac{w_n S_{MAX}}{\pi\,(n^2-1)} \cdot \eta \; q_o q_n \qquad \ldots\ldots(2.9)$$

The cutoff frequency of the diode is defined as:

$$F_c = \frac{1}{2\; C_{MIN} r_s} \quad * \qquad \ldots\ldots(2.10)$$

---

* see footnote of page 14.

letting $m = \dfrac{w_n(n^2 - 1)}{2w_c n}$ ....(2.11)

and $a = m + \sqrt{1 + m^2}$ ....(2.12)

then $an\sin(w_o t') - \sin(nw_o t') = \alpha$ ....(2.13)

where t' is time when total charge is a maximum (ie. $i = dq/dt$). By substitution:

$$P(w_o) = \frac{an^2 w_o q_B^2}{\alpha^2 n^2 C_{MIN}(n^2 - 1)} = \frac{an^2 w_o V_B^2 C_{MIN}}{\alpha^2 (n^2 - 1)} \quad \text{..............(2.14)}$$

---

* The diode acts as a source of power at the nth harmonic of the input frequency. These results are true only for a loss free diode and in order to take into account practical devices it is assumed the diode is represented by a constant loss resistance r_s in series with the variable junction capacitance. (Fig. 2.5)

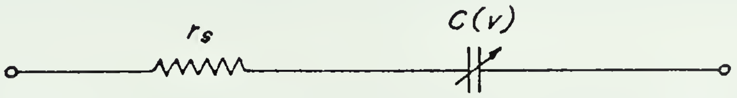


FIG. 2.5 Diode Equivalent Circuit

This theory was based on Judd's work(6) although others(7,8) have treated a similar case. Judd obtained reasonably good experimental verification. However, the following assumptions (made to simplify the analysis) will have undoubtedly contributed error:

(1) The diode switched with negligible transition time as a function of the input frequency.

(2) r_s, the series resistance or loss mechanism of the diode, is assumed to be constant. This is valid only in the high reverse or forward bias regions.

(3) For calculations of bias resistance, the linear recombination law is assumed ($i_{dc} = \bar{q}+/\tau$ where τ = minority carrier lifetime, and $\bar{q}+$ is the mean value of the positive half-cycle of the charge waveform for the step recovery diode).

2.3 Basic Design Techniques In Multi-Diode Harmonic Generators

High power frequency multipliers can be constructed with n diodes arranged in such a fashion that input and output power is shared equally among them. Several configurations or arrays utilizing more than one diode have been constructed to date with no appreciable loss in efficiency. A complete review of all of them will not be

attempted in the following discussion but rather an analysis of basic arrays which in turn can be combined to produce more intricate ones will be considered.

By connecting varactors in series (Fig. 2.6), the output power capability is increased over that of single devices. If n varactors are series connected, V_B increases by nV_B and C_o decreases by C_o/n. Thus the power handling capability has been increased by n.

$$P_r = \frac{C_o}{n} (nV_B)^2 = nC_oV_B^2 \qquad \ldots\ldots(2.15)$$

and the cutoff frequency $f_c = \frac{1}{2\ C_v r_s}$ has not been affected.*

In 1965 Irwin and Swan$^{(9)}$ examined series stacked assemblies with packaged varactors soldered together, one on top of the other. Full advantage of the series connection could not be obtained because heat could not be readily removed from the upper varactor. To utilize the increased power dissipation capability, all chips in the structure must be efficiently coupled to a heat sink. (Fig. 2.7)

---

* In the series connected or stacked varactor chip, r_s, the series resistance (semiconductor bulk and contact resistance) is increased by a factor "n". It is assumed that the interconnecting leads are of negligible resistance.

The number of chips which can be placed in a series connected varactor is limited by the physical dimensions of the package. When its size becomes appreciable with respect to a quarter wavelength at the operating frequency, unequal power distribution occurs. Arrays in which varactors are separated by phase shift networks are often used to overcome this difficulty(10,11). If networks with appropriate image impedances and equal phase shifts ϕ are placed between each diode as shown in Fig. 2.8, then, at the input frequency, all varactors will be matched and each will be driven by the same amount of power. At the output frequency (nF_o), each varactor works like a voltage source with $-n$ times the phase angle of its input voltage. If networks with appropriate image impedances and phase shifts of $+n\phi$ (at the output frequency) are placed between each diode, all output power from individual diodes appears at the load. As an example, the $\lambda/2$ type of array shown in Fig. 2.9 has been extensively used as a doubler (10,11). At the input frequency, power is shared equally among the diodes (Fig. 2.10). At $2F_o$, the output frequency, each varactor is electrically equivalent to a voltage source with 2x the phase angle of its input and a phase shift of λ between adjacent diodes (Fig. 2.11). Thus all output power from individual diodes appears at the load, when the varactors are perfectly matched.

Symmetry has also been utilized in arrays to

produce both even and odd order multipliers. Penfield and Rafuse's bridge circuit(12) is an effective even harmonic generator (Fig. 2.12) with four times the normal power handling capability, while Avellino's harmonic generator(13) (Fig. 2.13) is capable of producing only odd harmonics.

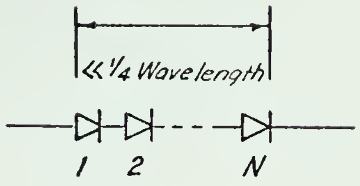


FIG. 2.6 SERIES CONNECTED VARACTOR CHAIN

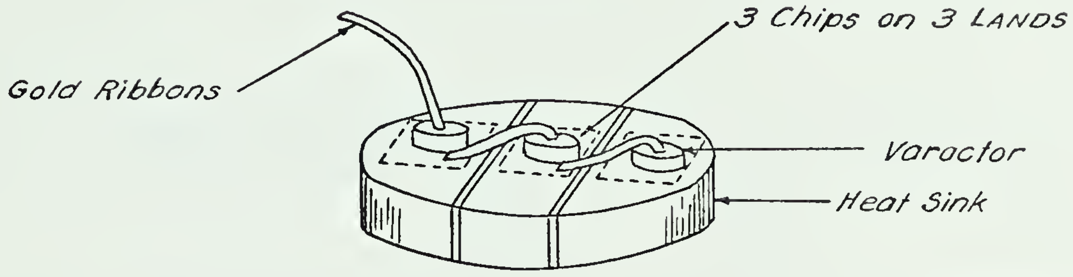
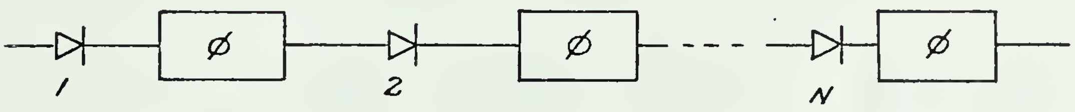
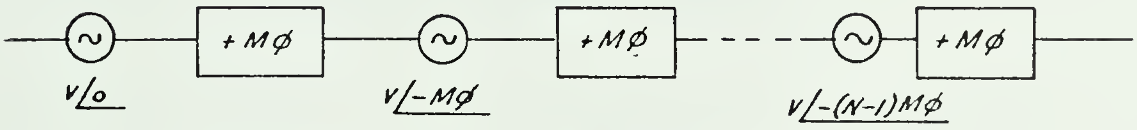


FIG. 2.7 THREE CHIP SERIES CONNECTED VARACTOR



Equivalent circuit at input frequency



Equivalent circuit at output frequency

FIG. 2.8 ARRAY IN WHICH VARACTORS ARE SEPARATED BY PHASE SHIFT NETWORKS

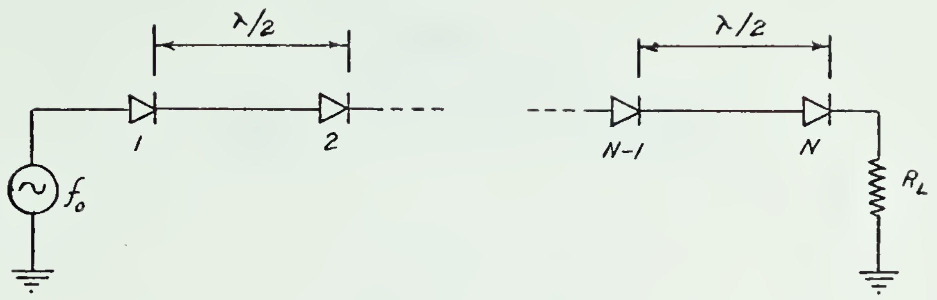


Fig. 2.9 $\lambda/2$ Phase shift array

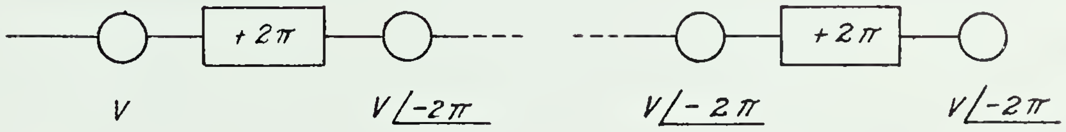


Fig. 2.10 Equivalent circuit for Fig. 2.9 at output frequency ($2f_o$)

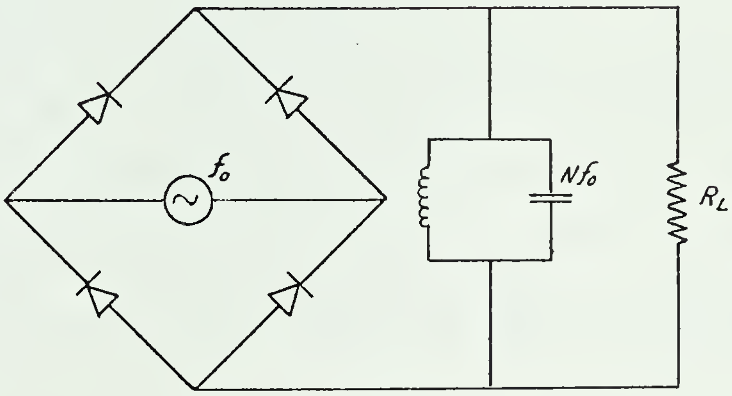


Fig. 2.11 Penfield's bridge circuit

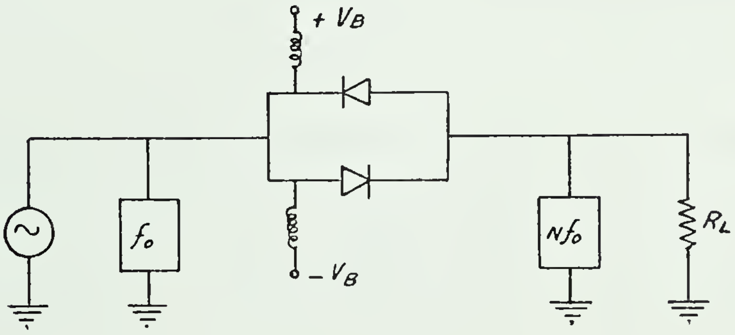


Fig. 2.12 Odd harmonic generation with opposingly biased diodes

CHAPTER III

The One-Diode Doubler

3.1 Introduction

In a frequency multiplier containing several diodes, tuning often becomes a tedious procedure as individual stages are coupled to one another. One method of overcoming this problem is the separate tuning of stages before final circuit assembly. However, the practical limitations of this method are obvious. Since high power multipliers employing several diodes were to be considered in this project, practical tuning techniques were of interest. To provide greater insight into this problem as well as the characteristics of the step recovery diode, the one diode doubler was initially considered.

Two such multipliers were constructed, one capable of matching over a wide range of impedances,(8) the other employing $\frac{1}{4}$ wavelength transformers. Strip transmission line was chosen for its relatively low cost, weight, size and ease in fabricating microwave circuits (14,15,16,17,18,19,20,21). The shunt, rather than the series configuration, was chosen for the following reasons:

(1) From a mounting standpoint (Fig. 3.2), the shunt configuration was more convenient and provided for efficient heat sinking.

(2) In the shunt arrangement, only currents at the fundamental and output frequency can flow through the diode, whereas in the series configuration, currents of the 2nd and all higher harmonics can flow. Thus in the latter case, losses will be greater and it is more difficult to separate desired and undesired frequencies.

3.2 Tunable Single Diode Doubler Design and Performance

Since the diode impedance was not known exactly, and since widely varying conditions of input power were to be examined, the system consisted essentially of a low loss stripline circuit capable of converting a wide range of impedances to 50Ω. The adaptation uses the principle that, for $\lambda/2$ length of line between the load and generator, perfect matching may be obtained with one shunt capacitance, variable in both magnitude and position on the line. This was accomplished by the use of tuning screws as illustrated in Fig. 3.3.

Single, open circuited stubs form simple input and output filters and isolate (to a first approximation)

the input and output (Fig. 3.4).

A seemingly more logical arrangement for single stub filtering would be attained by replacing stub (1) (Fig. 3.4) by a $\lambda/4$ stub (at 1GHz) terminated in a short circuit. The $\lambda/8$ stub was chosen for the following reasons:

(1) From bias considerations, it was necessary to isolate the short circuit if the $\lambda/4$ stub was incorporated.

(2) The $\lambda/8$ stub did not affect the real part of the impedance, but merely decreased the inductive reactance seen by the fundamental reactance at the stub intersection (Fig. 3.5).

The circuitry used to obtain experimental results is shown in Fig. 3.1, input versus output power in Fig. 3.6, output power versus frequency in Fig. 3.7, and both forward conduction current and output power versus bias voltage in Fig. 3.8.

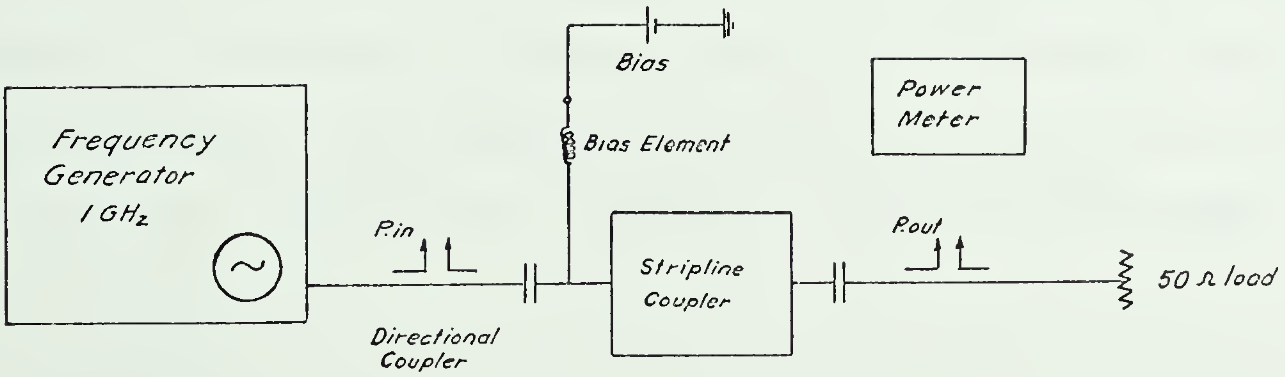


FIG. 3.1 Tunable Doubler Test Circuitry

Because the percentage of harmonic generation in the step recovery diode is not a significant function of signal level, but primarily of waveform, linear power characteristics, as verified in Fig. 3.6, are to be expected. In obtaining these results, only the bias was retuned. (Table 3.1) Output power ($P(w_o)$) as a function of bias (for maximum efficiency) is usually given by a relationship of the form:

$$P(w_o) = KV_B^2 C_{MIN} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.1)$$

Judd(6), Roulston(8) and others(7) have derived expressions of this form assuming the step recovery diode operation was based on two discrete states of reactance, and its ability to switch rapidly between these states. For bias levels sufficiently high that the reverse bias capacitance is relatively constant, the above expression holds (Table 3.1). However, for low bias levels where capacitance is not constant, poor agreement is obtained. The capacitance voltage characteristics for the Motorola IN5151(5) step recovery diode utilized are shown in Fig. 3.9. For reverse bias greater than 10V, capacitance is relatively constant. However, for the bias region $0 < V_B < 10$, the capacitance can be approximated as an exponential function of voltage of the form $C = KV^n$ ($C = 11.38V^{-.42}$PF. ±10%).

Power Out $P(w_o)$	Experimental Fixed Bias	Normalized Exp. Bias	$V_B = \sqrt{\frac{P(w_o)}{C_{MIN}}}$
.063	8.2	.766	.37
.21	8.9	.830	.69
.437	10.7	1	1
.58	12.0	1.12	1.15
.866	15.1	1.41	1.41
1.98	21.8	2.02	2.16
2.42	27.0	2.53	2.39

TABLE 3.1 Relationship Between Bias And Output Power

Output power versus frequency for the fixed tuned case is shown in Fig. 3.7. A 3db bandwidth of approximately 2.5% was obtained with output isolation of the fundamental (F_o) in the order of 15db. By increasing the bias for a constant input signal, the input output isolation was decreased. This is indicated in Fig. 3.8, where for bias levels greater than or equal to 19 volts, output power is of the fundamental frequency. At this bias level, forward conduction ceased, indicating that the diode was no longer operating in the charge storage mode.

Biasing of the step recovery diode may be accomplished in one of two ways, self bias using a resistor, or fixed bias with an external power supply.

The latter was used to obtain experimental data. Self bias has the advantages of low cost, a degree of temperature compensation, and self-adjustment for different input levels, its only disadvantage being that diode variation will necessitate different values of bias resistance if optimum performance is required. A comparison of the two techniques with respect to efficiency is shown in Fig. 3.10. A one megohm potentiometer was used as the bias resistor.

3.3 Proposed Method For Tuning n Diode Multipliers

Recombination, due to a finite minority carrier, lifetime τ, is the major mechanism responsible for leakage current in the step recovery diode. As a first approximation the direct current flowing in the bias circuit is given by: $i_{DC} = \frac{\overline{q}+}{\tau}$ where $\overline{q}+$ is the mean value of the positive half cycles of the charge waveform for the step recovery diode. Considering a typical current waveform for the step recovery diode (Fig. 3.11), the following relationship must hold:

$$\int_{0}^{t_1} idt - \int_{0}^{t_1} i_{recomb} - \int_{t_2}^{t_3} idt = 0$$

It is assumed that charge storage under reverse bias condition is negligible.

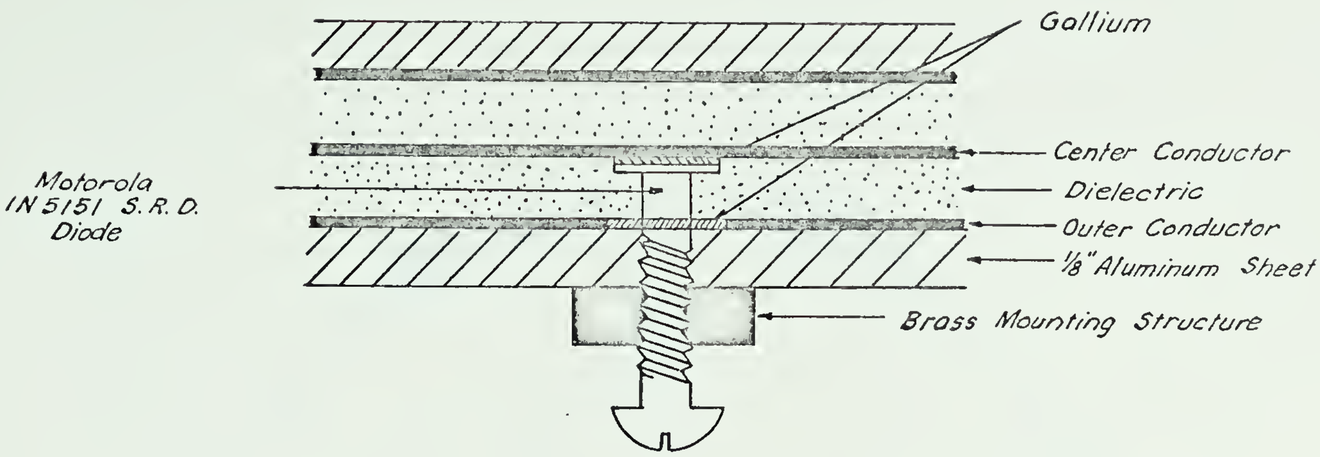


FIG. 3.2 DIODE STRIPLINE MOUNT - SHUNT CONFIGURATION

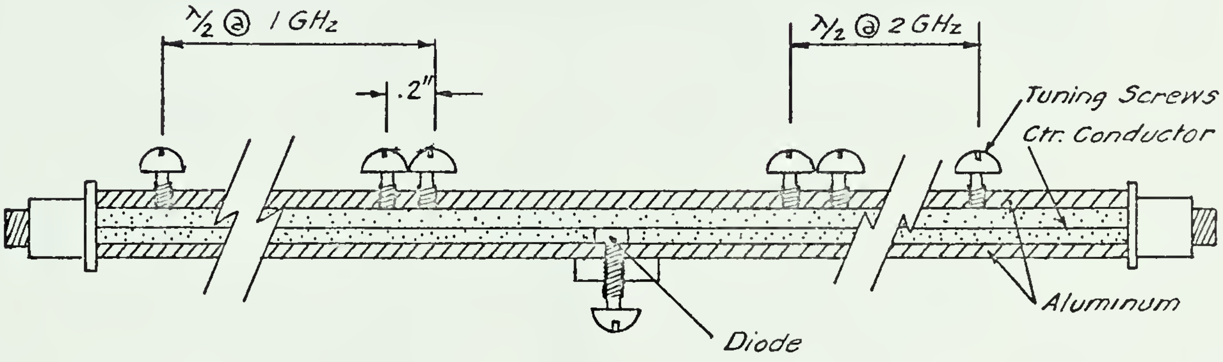
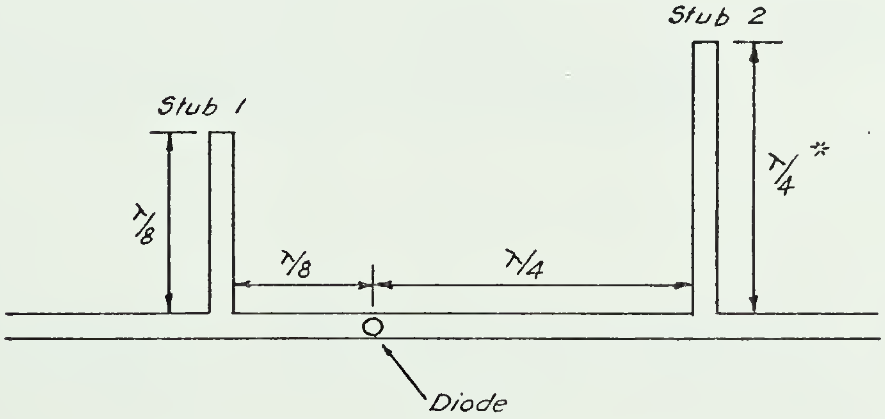
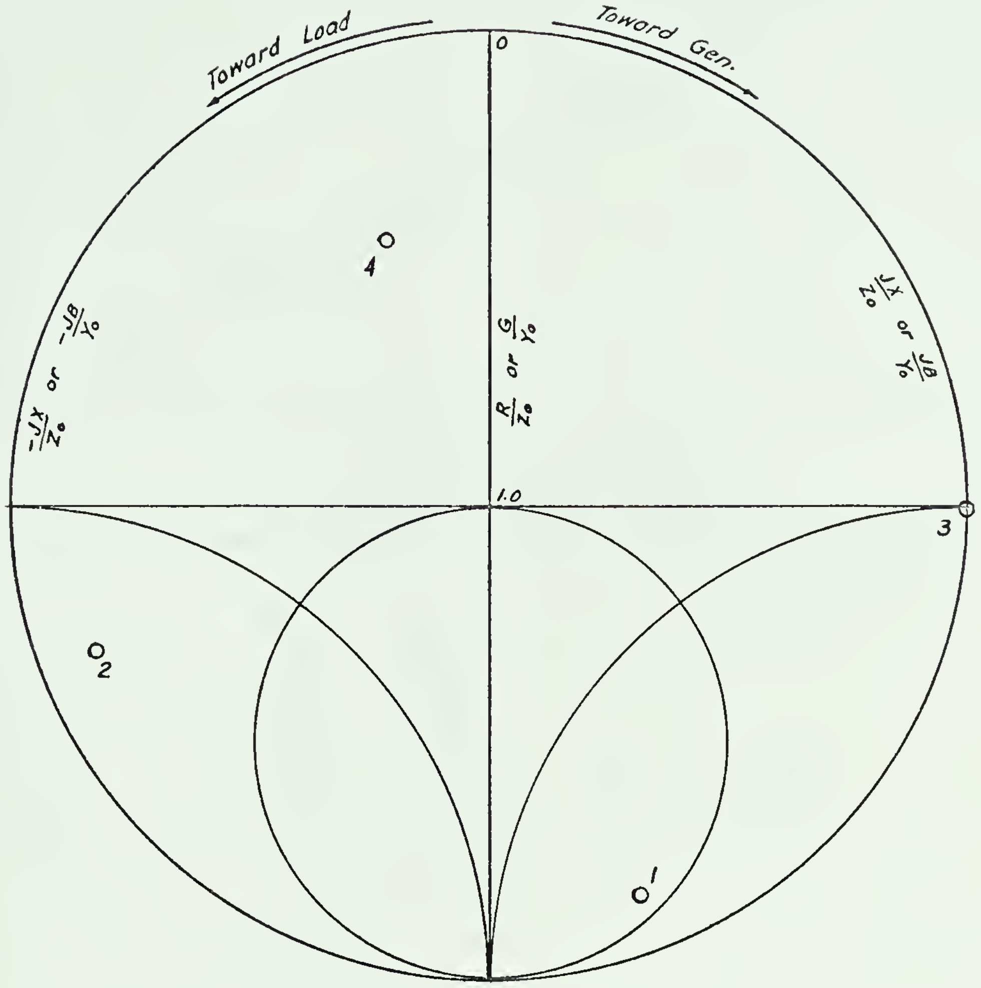


FIG. 3.3 MATCHING SYSTEM EMPLOYING TUNING SCREWS



* All distances shown are w.r.t. 1 GHz

FIG. 3.4 SINGLE STUB FILTERING NETWORK (TOP VIEW - CENTER CONDUCTOR)


Toward Load
Toward Gen.
0
$-\frac{jX}{Z_0}$ or $-\frac{jB}{Y_0}$
$\frac{R}{Z_0}$ or $\frac{G}{Y_0}$
$\frac{jX}{Z_0}$ or $\frac{jB}{Y_0}$
1.0
1
2
3
4

① Approx. diode admittance at fundamental.

② Diode admittance transformed to stub ①

③ Admittance of stub ① at fundamental frequency.

④ Admittance seen by generator at stub intersection

(ie Admittance ④ = Admittance ② + ③)

Fig. 3.5 Effect of $\lambda/8$ stub (w.r.t. fundamental frequency)

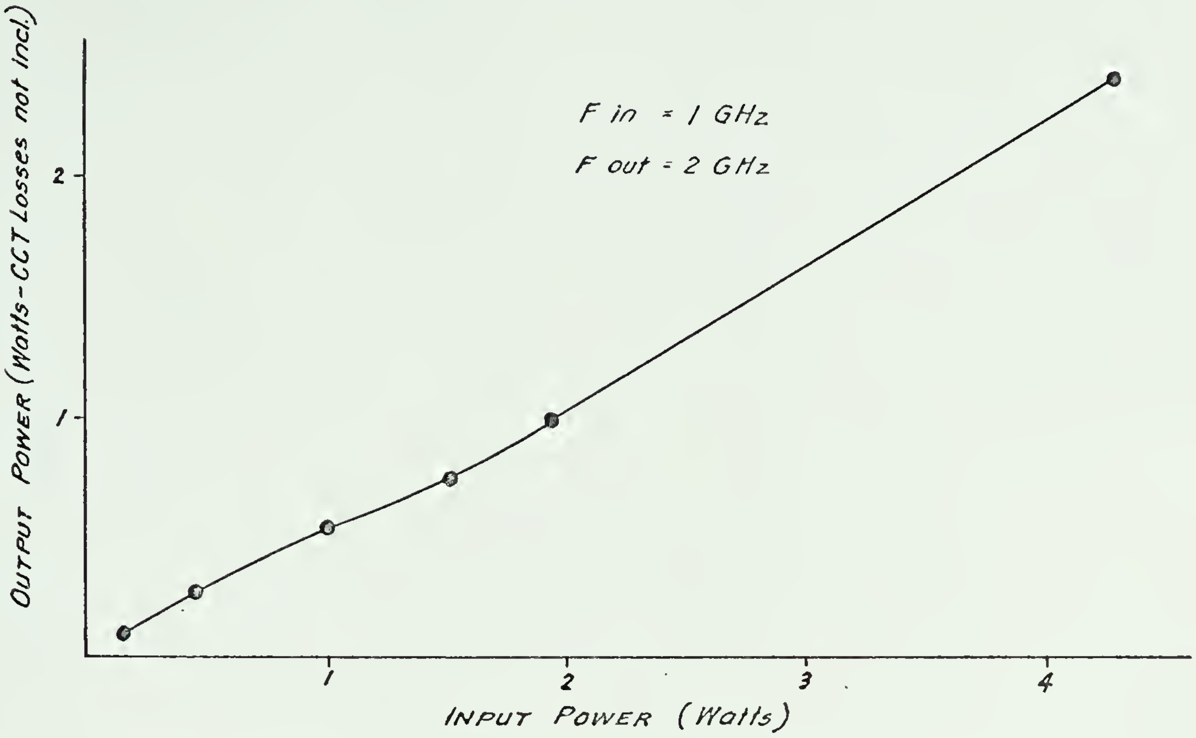


FIG. 3.6 INPUT VS OUTPUT POWER IN WATTS (TUNABLE DOUBLER)

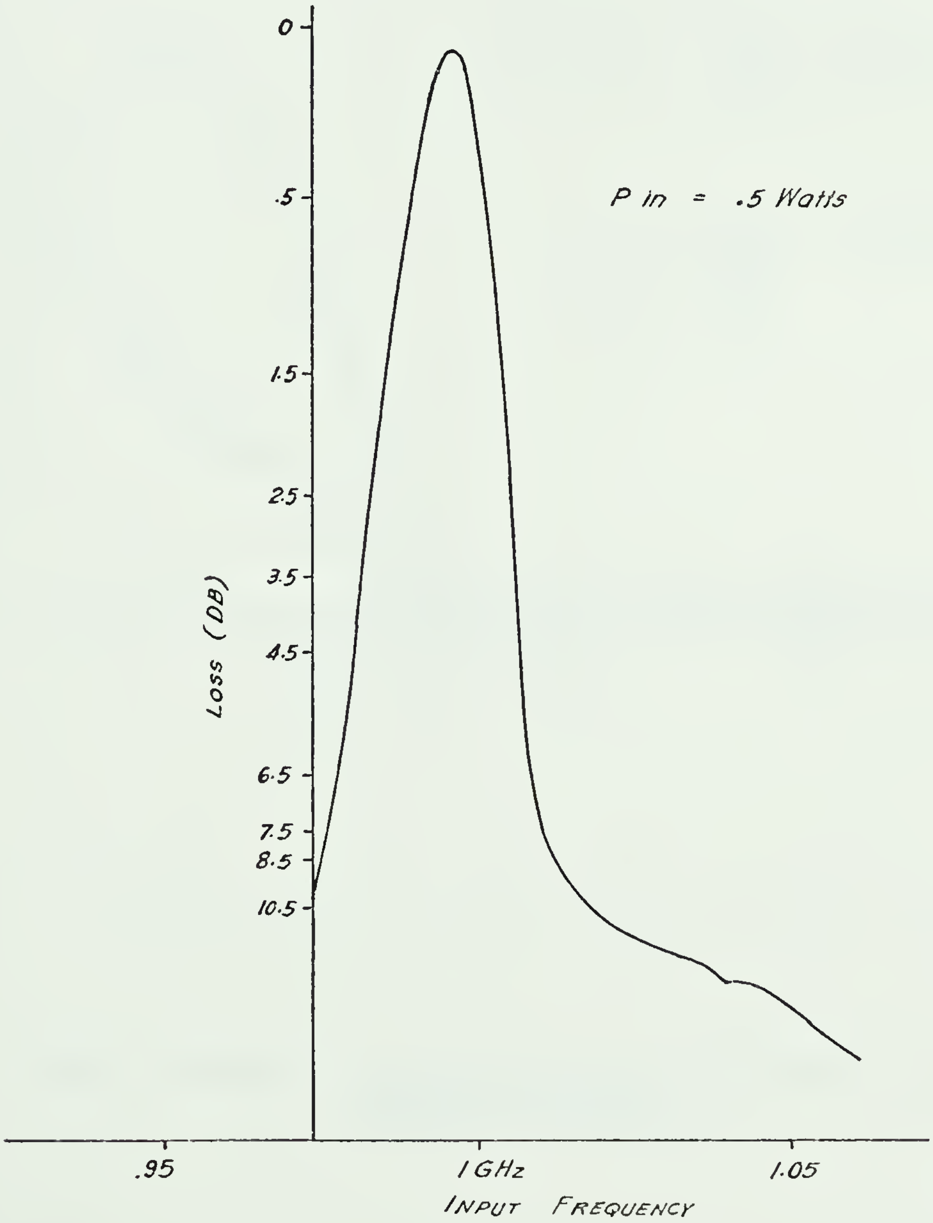


FIG. 3.7 OUTPUT POWER VS FREQUENCY FOR TUNABLE DOUBLER (NO RETUNING)

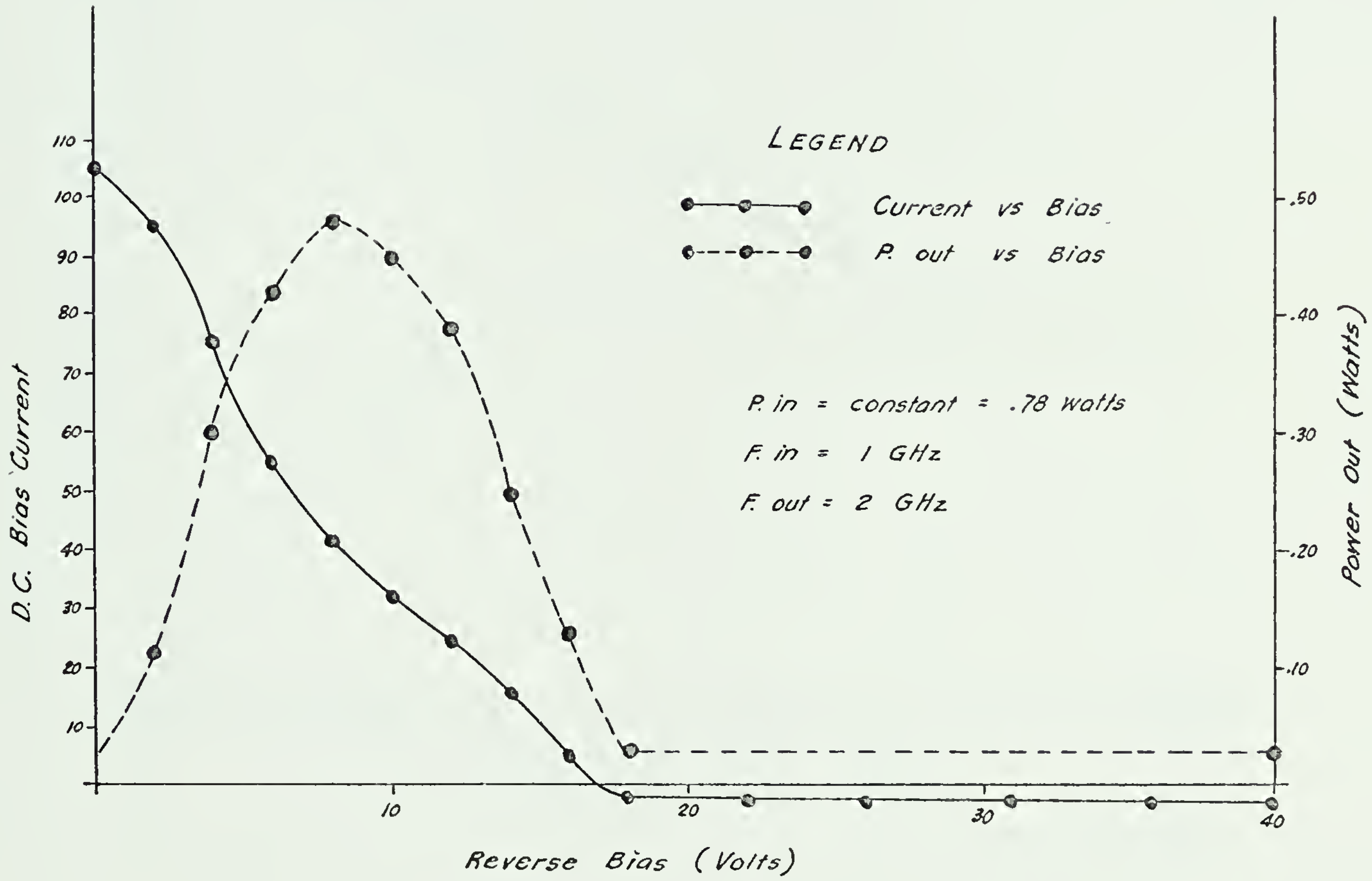


FIG. 3.8 BIAS CURRENT AND POWER OUTPUT VS BIAS VOLTAGE FOR TUNABLE DOUBLER

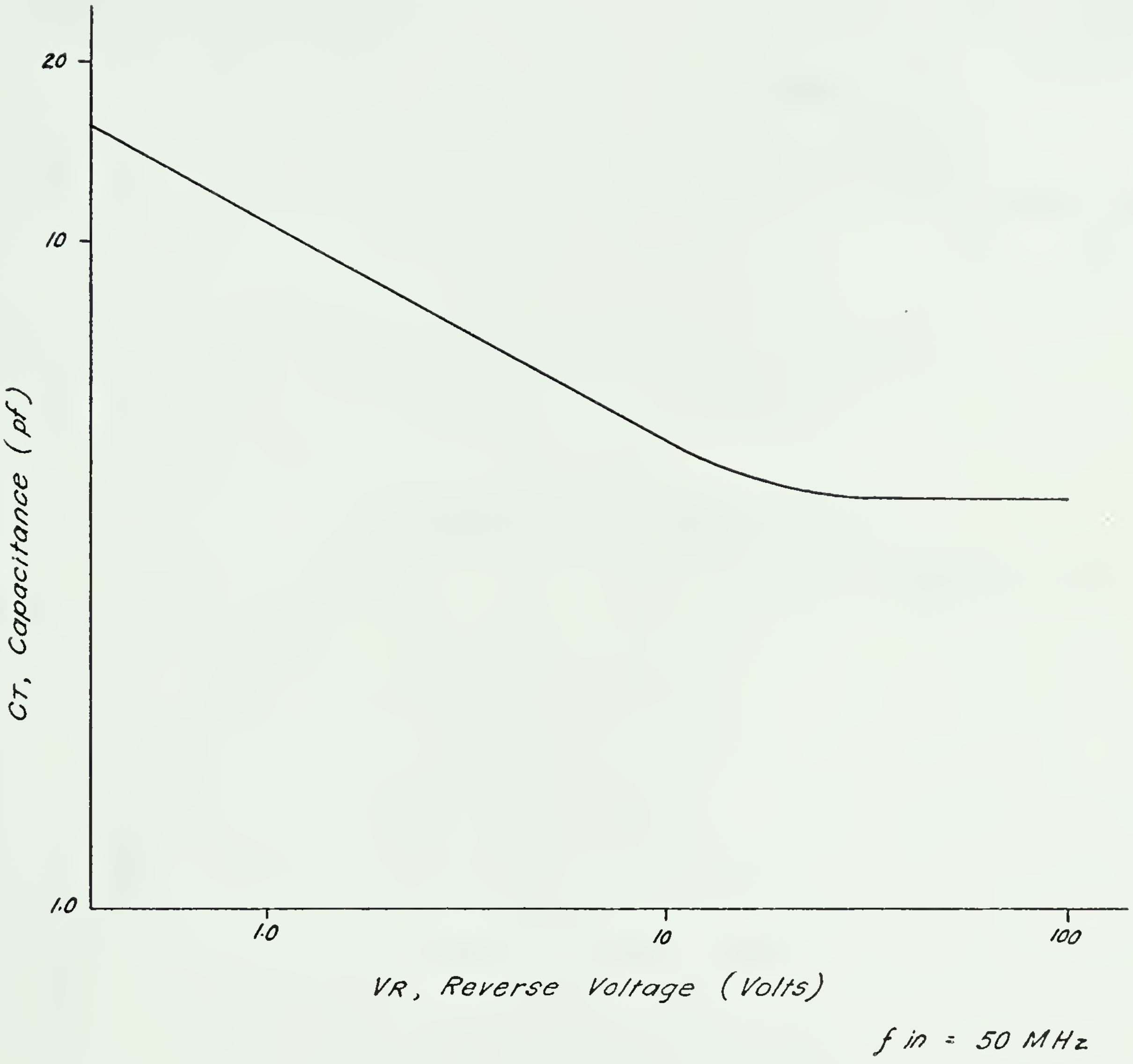


FIG. 3.9 VARACTOR CAPACITANCE VERSUS REVERSE VOLTAGE FOR MOTOROLA IN5151 STEP RECOVERY DIODE.

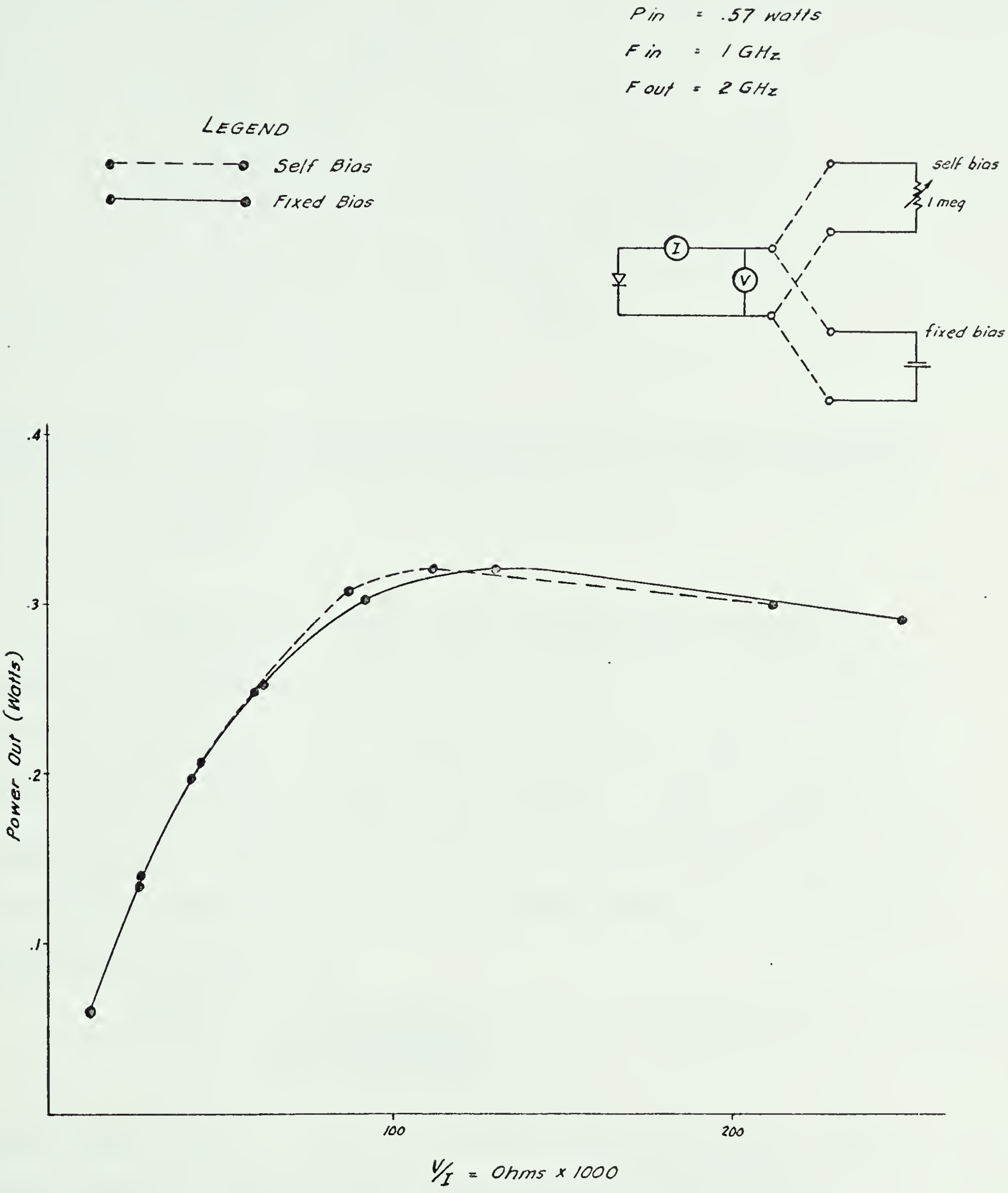


FIG. 3.10 COMPARISON OF FIXED AND SELF BIAS

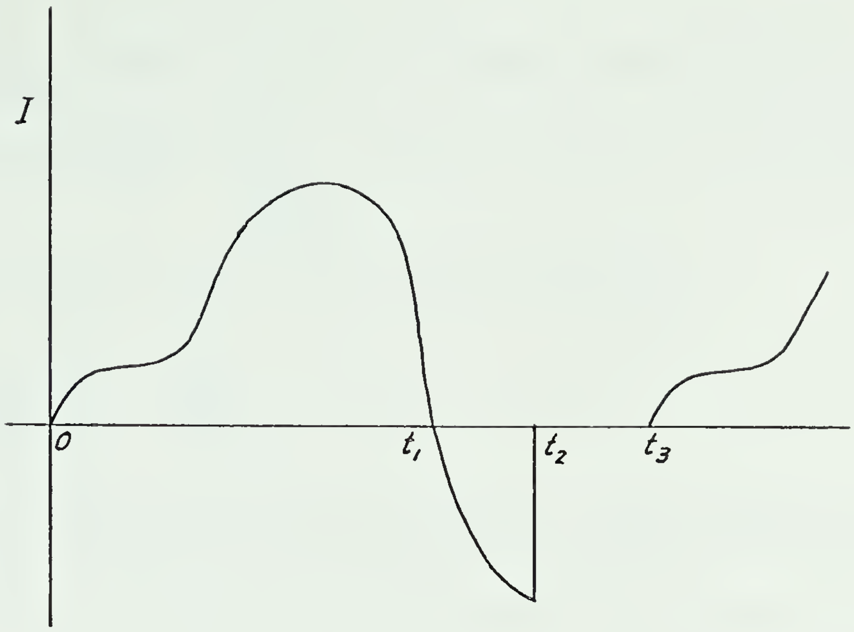


FIG. 3.11 Typical Current Waveform For A Step Recovery Diode

Figure 3.8 shows the variation of forward conduction current in the bias circuit, as a function of the bias voltage. For optimum efficiency there exists a particular bias voltage and current. Their product is a maximum for maximum efficiency as predicted from Judd's theory(6). From Section 2.2, output power in a harmonic generator is given by

$$P(w_o) = \frac{a n^2 w_o V_B{}^2 C_{MIN}}{\pi \alpha^2 (n^2 - 1)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.2)$$

Since $i_{DC} = \bar{q}+/\tau$ assuming linear recombination, then the average voltage across the diode is given by:

$$V_C = S_{MAX}\bar{q}+ \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.3)$$

Since $V_C = i_{DC} r_B$ where r_B is the bias resistance, then:

$$r_B = S_{MAX}\tau = \frac{\tau}{C_{MIN}} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.4)$$

Substituting (3.4) into (3.2) one obtains:

$$P(w_o) = \frac{a^2 w_o \tau n^2}{\pi \alpha^2 (n^2-1)} \; \frac{V_B^2}{r_B} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.5)$$

From data (obtained either experimentally or mathematically) correlating both optimum bias voltage and current to various input power levels, one would have two parameters (bias voltage and current) to tune individual varactors in a chain. The following method is proposed to provide greater ease in tuning an n-diode array:

(1) From diode data, set the optimum bias voltage if fixed bias is employed or the optimum resistive value for the self bias case, for the expected power level incident on each diode.

(2) Proceed to tune the interstage coupling networks between the diodes such that the desired forward conduction current in each diode occurs. This method makes it immediately apparent if a diode is being either over or under driven. In the former case, the conduction current will be greater than expected whereas in the latter, the opposite is true. This fact is illustrated in Figure 3.8. By decreasing the bias (effectively increasing the input signal), forward conduction current

increased. By increasing bias (effectively reducing incident power), conduction current decreased until finally the diode was operating completely in the reverse bias region.

This technique is also useful if additional diodes are to be employed as matching or switching devices in a multiplier. By monitoring the leakage current (direction and magnitude), it becomes apparent if the device is operating in its intended fashion.

The above method by no means makes tuning of long varactor chains a trivial task. However, by monitoring the forward conduction current in each diode, the effect of tuning a particular interstage coupling network on power levels at other diodes in the circuit becomes immediately visible. Incorrect tuning of a particular stage in a multiplier would become apparent as bias currents elsewhere in the circuit would deviate considerably from their expected values.

3.4 A Narrowband Single Diode Doubler

The tunable doubler (Sect. 3.2) was useful for experimental purposes because of its versatility in matching over a wide impedance range. However, when the diode impedance is known, it is customary to use matching elements such as π sections or quarter wave transformers(21). These matching devices are usually employed in commercial multipliers for reasons of economy and construction ease. It was thus of interest to construct a frequency multiplier incorporating fixed matching devices.

In order to design matching networks between the source, diode, and load, it is necessary to know the input and output impedance of the device under the expected operating conditions. Although work in this area has been done, it is difficult to predict, theoretically, the exact impedances as the step recovery diode mechanism (22,23) is not completely understood. The values for diode impedance were taken from the manufacturers' data (5). Quarter wavelength transformers were employed as matching devices, strip transmission line was utilized, the diode mounting scheme being the same as in Fig. 3.2.

3.5 Derived Narrowband Doubler Design Equations And Results

A simplified multiplier circuit is shown below (Fig. 3.12).

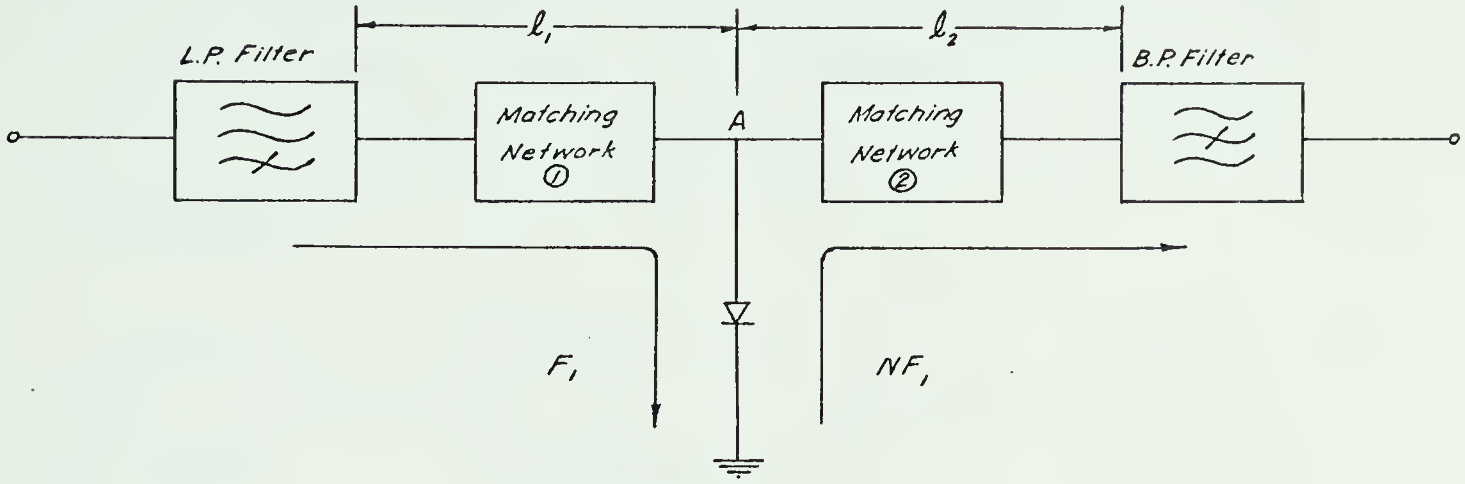


FIG. 3.12 Simplified Multiplier Circuit

When designing matching sections (1) and (2), consideration must be given to the out-of-pass band impedances contributed by the filters. For example, the bandpass filter, at the fundamental frequency, will have some impedance (essentially reactive) X_1. The impedance seen at A by the fundamental will be the diodes in parallel with X_1', the transformed filter impedance. It is advantageous to choose l_2 such that X_1' is ∞, as the effect of changes in filter characteristics due to aging, input power level, frequency shift, etc., is reduced when the diode impedance is small.

The stripline circuit (center conductor shown) in Fig. 3.13 will be considered, the above requirements

being satisfied by proper choice of circuit geometry. Although a doubler is designed, the method can be extended to higher-order multipliers with the inclusion of the necessary idlers. The analysis presented holds for any type of diode as arbitrary dynamic impedance is assumed.

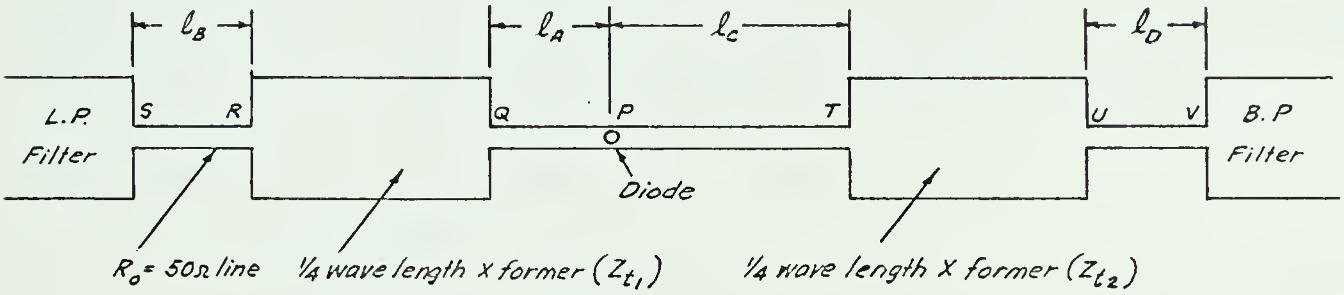


FIG. 3.13 Stripline Design For Narrowband Doubler (Top View Of Ctr. Conductor)

The list of symbols is given below.

B_1 = phase velocity in stripline of fundamental (w_o)

B_2 = phase velocity in stripline of first harmonic ($2w_o$)

$R_1 + jX_1$ = diode impedance at fundamental (w_o)

$R_2 + jX_2$ = diode impedance at first harmonic ($2w_o$)

X_{F1} = band pass filter impedance at w_o

X_{F2} = lowpass filter impedance at $2w_o$

Z_{T1} = impedance of $\frac{1}{4}(w_o)$ wavelength transformer

Z_{T2} = impedance of $\frac{1}{4}(2w_o)$ wavelength transformer

Distance l_A and the input quarter wavelength transformer will be considered initially (Fig. 3.13). Distance l_A must be chosen such that the diode impedance (seen by the fundamental at P) transforms to some real value at Q, R_Q. Input matching will then be achieved by making the quarter wavelength transformer impedance, Z_{T1}, the square root of the product of R_Q and 50Ω. Ignoring the effect of the bandpass filter, the diode impedance seen by the fundamental at P is:

$$Z_P = R_1 + jX_1 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.6)$$

This impedance transformed to Q will assume a value R_Q such that

$$R_Q = R_0 \frac{(R_1 + jX_1)\cos B_1 l_A + jR_0 \sin B_1 l_A}{R_0 \cos B_1 l_A + j(R_1 + jX_1)\sin B_1 l_A} \quad . (3.7)$$

equating real and imaginary parts

$$R_Q = \frac{R_1^2 + R_0^2 + X_1^2 \pm (R_1^2 + R_0^2 + X_1^2)^2 - 4R_1^2 R_0^2}{2R_1} \quad \ldots\ldots\ldots (3.8)$$

$$l_A = \frac{1}{B_1} \tan^{-1} \frac{X_1 R_0}{R_Q R_1 - R_0^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.9)$$

input matching will be accomplished when

$$Z_{T1} = \sqrt{50R_Q} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.10)$$

Two choices for R_Q are available, the smaller being preferable as the quarter wavelength transformer will have least loss.(24)

A similiar method is used to determine l_C and

Z_{T2}, the only difference being that the diode is considered as the source rather than the load. In this case, the general lossless impedance formula assumes the form

$$Z_2 = R_0 \frac{Z_1 \cos bl - jR_0 \sin bl}{R_0 \cos bl - jZ_1 \sin bl} \quad \ldots\ldots\ldots\ldots (3.11)$$

solving for l_C and Z_{T2}

$$R_T = \frac{R_2^2 + R_0^2 + X_2^2 \pm (R_2^2+R_0^2+X_2^2)^2 - 4R_2^2R_0^2}{2R_2} \quad \ldots\ldots (3.12)$$

$$l_C = \frac{1}{B_2} \tan^{-1} \frac{X_2 R_0}{R_T R_2 - R_0^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.13)$$

$$Z_{T2} = \sqrt{50R_T} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.14)$$

Thus far, the effect of additional impedance contributed by the filters has been ignored. Proper choice of l_B and l_D ensure this assumption is valid.

The distance l_D will be considered initially. At the fundamental, the bandpass filter has some reactance jX_1 associated with it. Transforming this reactance to P must produce an open circuit. Thus the impedance seen at P by the fundamental will be the diodes with no contribution from the filter. Assuming this condition exists, (Fig. 3.14) then

$$Z_{PT} = \infty \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.15)$$

transforming to T

$$Z_T = j \frac{R_0}{\tan B_1 l_C} = jR_T \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.16)$$

Transforming to point U

$$Z_U = jZ_{T2} \frac{R_T - Z_{T2}}{Z_{T2} + R_T} = jR_B \quad \ldots\ldots\ldots\ldots\ldots(3.17)$$

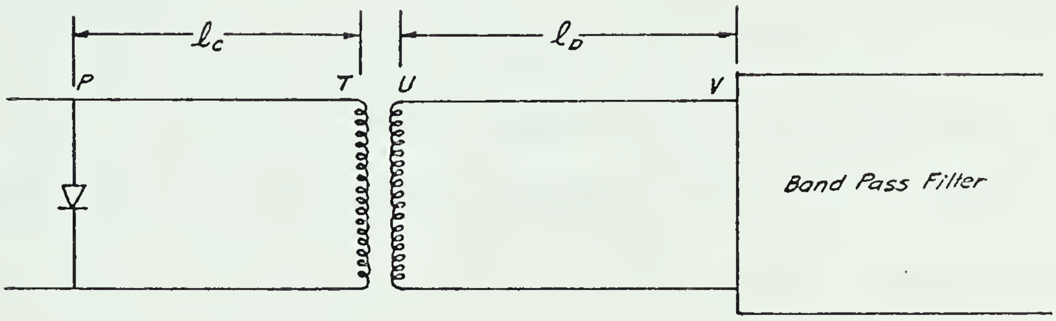


FIG. 3.14 Output Matching Section For Narrowband Doubler

Finally, the following condition must exist if the assumption that jX_1 transforms to an open circuit at the diode junction is to be valid:

$$jX_{F1} = R_0 \frac{jR_B - jR_0 \tan B_1 l_D}{R_0 + R_B \tan B_1 l_D} \quad \ldots\ldots\ldots\ldots\ldots(3.18)$$

Solving for l_D

$$l_D = \frac{1}{B_1} \tan^{-1} \frac{R_0 R_B - X_{F1} R_0}{X_{F1} R_B + R_0^2} \quad \ldots\ldots\ldots\ldots\ldots(3.19)$$

where $R_B = Z_{T2} \dfrac{\dfrac{R_0}{\tan B_1 l_C} - Z_{T2}}{Z_{T2} + \dfrac{R_0}{\tan B_1 l_C}} \quad \ldots\ldots\ldots\ldots\ldots(3.20)$

Using a similar technique for obtaining l_B one obtains

$$l_B = \frac{1}{B_2} \tan^{-1} \frac{R_0 R_Q^1 - X_{F2} R_0}{X_{F2} R_Q^1 + R_0^2} \quad \ldots\ldots\ldots\ldots\ldots\ldots (3.21)$$

where $$R_Q^1 = \frac{R_0}{\tan B_2 l_A} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.22)$$

Utilizing these design equations (3.9, 3.10, 3.13, 3.14, 3.19, 3.21) and empirical formulas derived from manufacturers data for optimum input and output impedance, the 2nd doubler was constructed. Reasonable agreement was obtained w.r.t. optimum input impedance between Judd's(6) theory and Motorola data(5). However, there was a large discrepancy between output impedances. Applying Judd's theory to the Motorola IN5151 step recovery diode:

$$w_C = \frac{1}{C_{MIN} r_s} = \frac{1}{4 \times 10^{-12} \times .5} = 5 \times 10^{11} \text{rad/sec} \quad \ldots\ldots (3.23)$$

$$M = \frac{w_n (n^2 - 1)}{2 w_C n} = 5.9 \times 10^{-2} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.24)$$

$$a = M + \sqrt{1 + M^2} = 1.059 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.25)$$

$$R_{IN} = s\left(1 + \frac{1}{aM}\right) = 8.5 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.26)$$

$$R_{out} = \frac{s}{M} \quad 1 + M^2 \quad = 8.47 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.27)$$

From Motorola data:

$$R_{IN} = \frac{45}{C_{MIN} f_{IN}} = 11.2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.28)$$

$$R_{out} = \frac{70}{C_{MIN} f_{IN}} = 17.5 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots (3.29)$$

No reasonable explanation for the large discrepancy in output impedances has been found.

The input lowpass, and output bandpass filters were of stripline construction providing 40db out-of-passband attenuation. Their design and performance are given in Appendices I and II respectively.

The circuitry used to obtain experimental results and the equivalent circuit for the multiplier and filters are shown in Figures 3.15 and 3.16 resp. An efficiency of 52% rather than the expected 58% was achieved, the discrepancy probably being produced by error in the assumed dynamic impedance of the diode. The dimensions (stripline center conductor) of the narrowband doubler are given in Fig. 3.17.

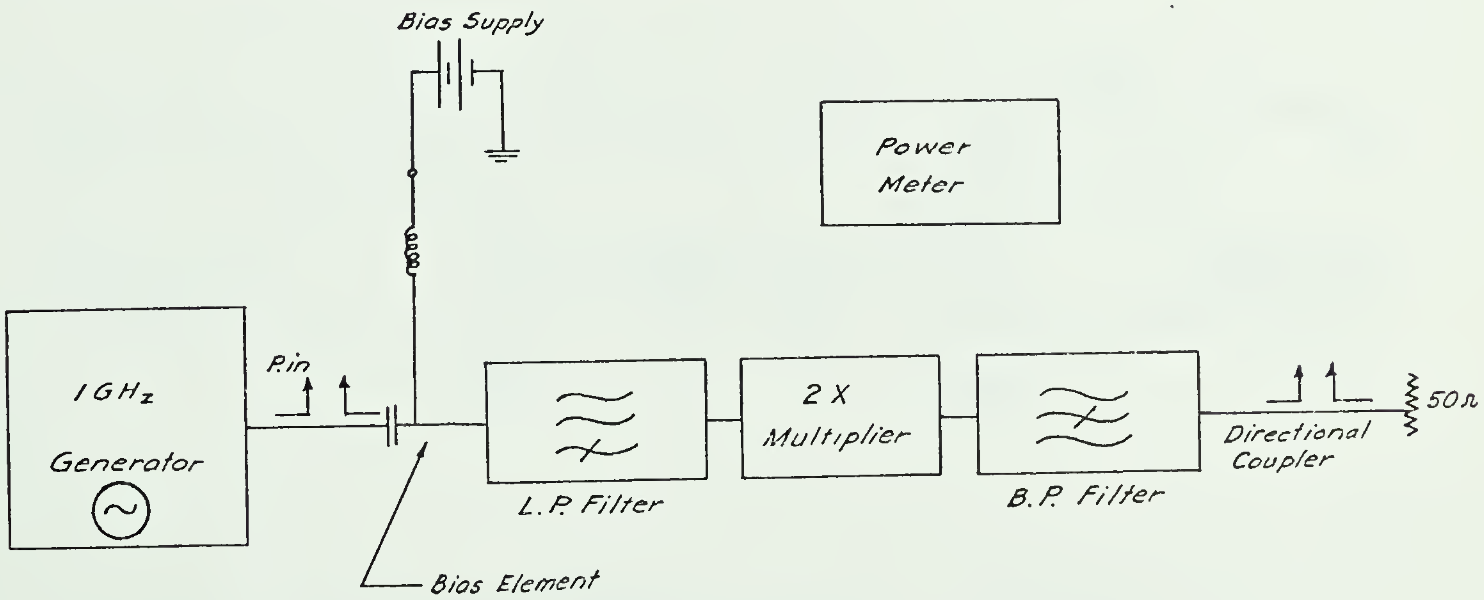


FIG. 3.15 Narrowband Doubler Test Circuitry

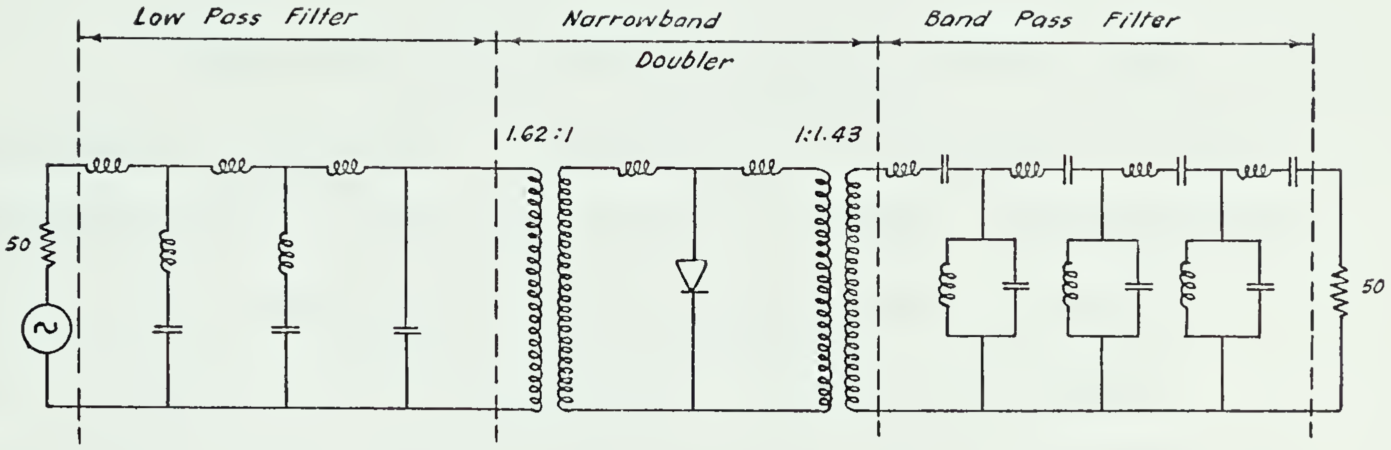


Fig. 3.16 EQUIVALENT CIRCUIT FOR THE NARROWBAND DOUBLER AND INPUT AND OUTPUT FILTERS

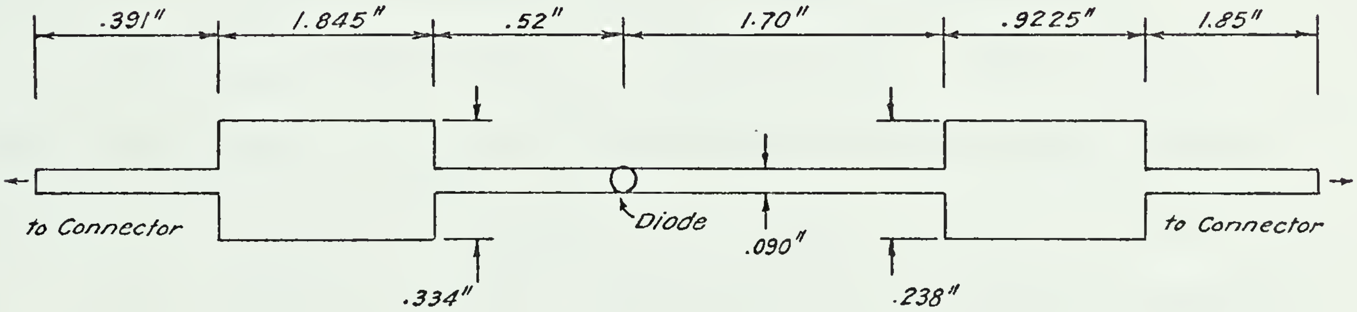


Fig. 3.17 DIMENSIONS (STRIPLINE CENTER CONDUCTOR) OF NARROWBAND DOUBLER

CHAPTER 4

4.1 High Power Doublers

One of the most common arrays in high power multipliers utilizes $\lambda/2$ spacing of the diodes (at the fundamental) in either the series or shunt configuration (Sec. 2.3). When the diodes have the same impedance with respect to the fundamental, output and idling frequencies, individual output power from the diodes is summed at the load. However a diode mismatch results in unequal input power distribution and output phase which both tend to decrease efficiency. This effect will be considered by analysing the two diode doubler shown in Fig. 4.1.

The step recovery diode can be treated as a switch, 'on' under forward bias or when containing stored carriers, and 'off' at other times. Let it be assumed therefore, that the switching action takes place between two states of linear resistance, r_f when turned on and r_b when turned off(7). Considering the shunt harmonic generator shown in Fig. 4.1, the diode currents, i_{d1} and i_{d2}, are restricted by the tuned circuits to be made up of only two frequency components at the input and desired harmonic frequency:

$$i_{d1} = i_0 e^{jwt} + i_0^* e^{-jwt} + i_M e^{jMwt} + i_M^* \, e^{-jMwt} \qquad .....(4.1)$$

$$i_{d2} = i_0{'} e^{jwt'} + i_0^{*}{'} e^{-jwt'} + i_M{'} e^{jMwt'} + i_M^{*}{'} e^{-jMwt'} \qquad ......(4.2)$$

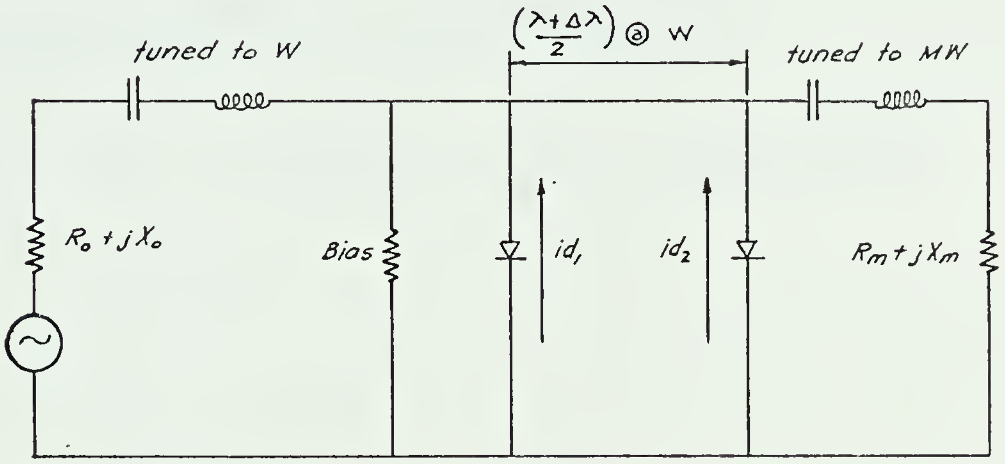


FIG. 4.1 Two Diode (λ/2 Spaced) Harmonic Generator

The time of switching may be related to the current waveform by phase angles Ø and θ so that the time variation of the diodes becomes

$$r_{d1}(t) = \sum_{M=-\infty}^{+\infty} r_M e^{jM(wt + \emptyset)} \qquad ....(4.3)$$

$$r_{d2}(t') = \sum_{M=-\infty}^{+\infty} r_M' e^{jM(wt' + \theta)} \qquad ....(4.4)$$

Considering i_0 and i_0', respectively, to be the phase reference, they may be defined as even functions. (ie) $i_0 = i_0^*$ and $i_0' = i_0^{*\prime}$. Therefore, multiplying equations (4.1) and (4.3), and (4.2) and (4.4) together (ignoring frequencies at the fundamental) gives the output voltages across diodes one and two respectively.

$$V_{d1} = i_0(r_{M-1}e^{j\overline{M-1}\phi} + r_{M+1}e^{j\overline{M+1}\phi})e^{jMwt}$$

$$+ i_M(R_M + jX_M + r_0)e^{jMwt} + i_M^*(r_{2M}e^{j2M\phi})e^{jMwt}$$

$$= (A + B + C)e^{jMwt} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots(4.5)$$

$$V_{d2} = (E + F + G)e^{jMwt'} \qquad \ldots\ldots\ldots\ldots\ldots\ldots\ldots(4.6)$$

Since the separation between the diodes was assumed to be $\frac{\lambda + \Delta\lambda}{2}$, this is equivalent in the time domain to $\frac{\pi + \Delta\pi}{w}$. Thus $t' = t + \frac{\pi + \Delta\pi}{w}$. Transforming V_{d1} to V_{d2} and summing them, the output voltage will be

$$V_0 = (A + B + C)e^{jMw(t' - \frac{\pi + \Delta\pi}{w})} + (E + F + G)e^{jMwt'}$$

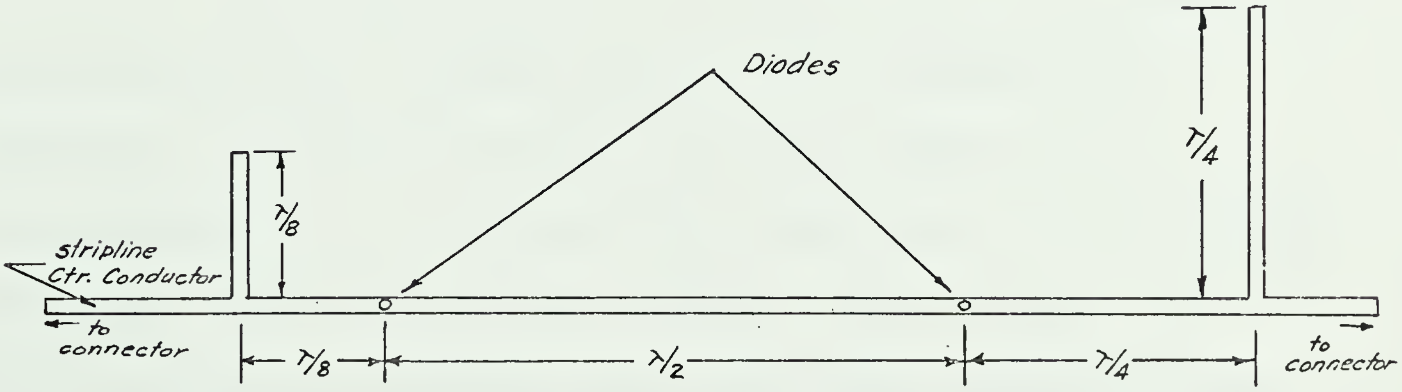
$$\ldots\ldots\ldots(4.7)$$

When $\Delta\pi = 0$ (exact $\lambda/2$ separation) and $A = E$, $B = F$, and $C = G$ (perfectly matched diodes), the output will contain equal contribution from both diodes, the efficiency being comparable to the one diode case and the power handling capability doubled.

For the case of diodes having unequal reactive

and or resistive components, $\Delta\pi \neq 0$ as the phases of the output voltages are not equal. Also, power distribution would not be equal, and $(A + B + C) \neq (E + F + G)$, thus reducing efficiency.

The stripline, two diode, shunt configuration multiplier constructed and the test circuit utilized in obtaining experimental results are shown in Figures 4.2 and 4.3 respectively. Input and output matching was accomplished with double stub tuners; filtering using the single stub method described in Section 3.2. Tuning screws (non symmetric) were inserted between the diodes to ensure $\lambda/2$ spacing between them. The diodes shared a common bias.



* All distances shown are w.r.t. 1 GHz

FIG. 4.2 Two Diode, Shunt Configuration Doubler (Center Conductor)

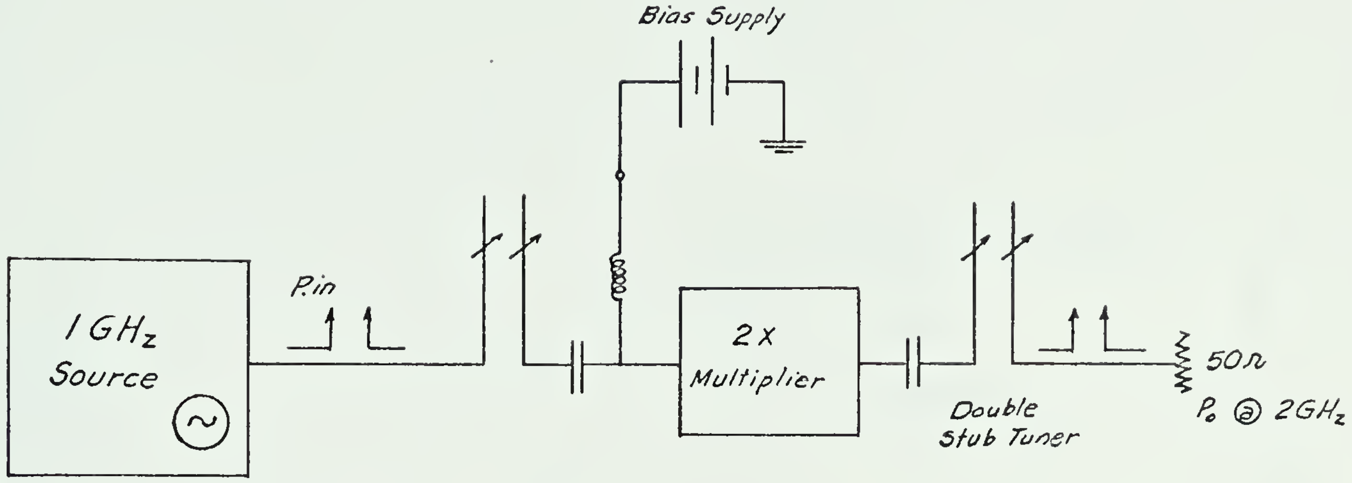


FIG. 4.3 Two Diode (λ/2 Spaced) Doubler Test Circuitry

An efficiency of 54% (Fig. 4.5) as opposed to 58% for the broadband single diode doubler was achieved. The additional loss would seem to be attributable to the common bias technique. If the diodes had been isolated from one another (with respect to D.C.) the bias voltages could have been separately adjusted for optimum performance. (For a given incident power level, the optimum bias voltage would differ slightly on the two diodes as they were not perfectly matched.) Variation of output power with forward conduction

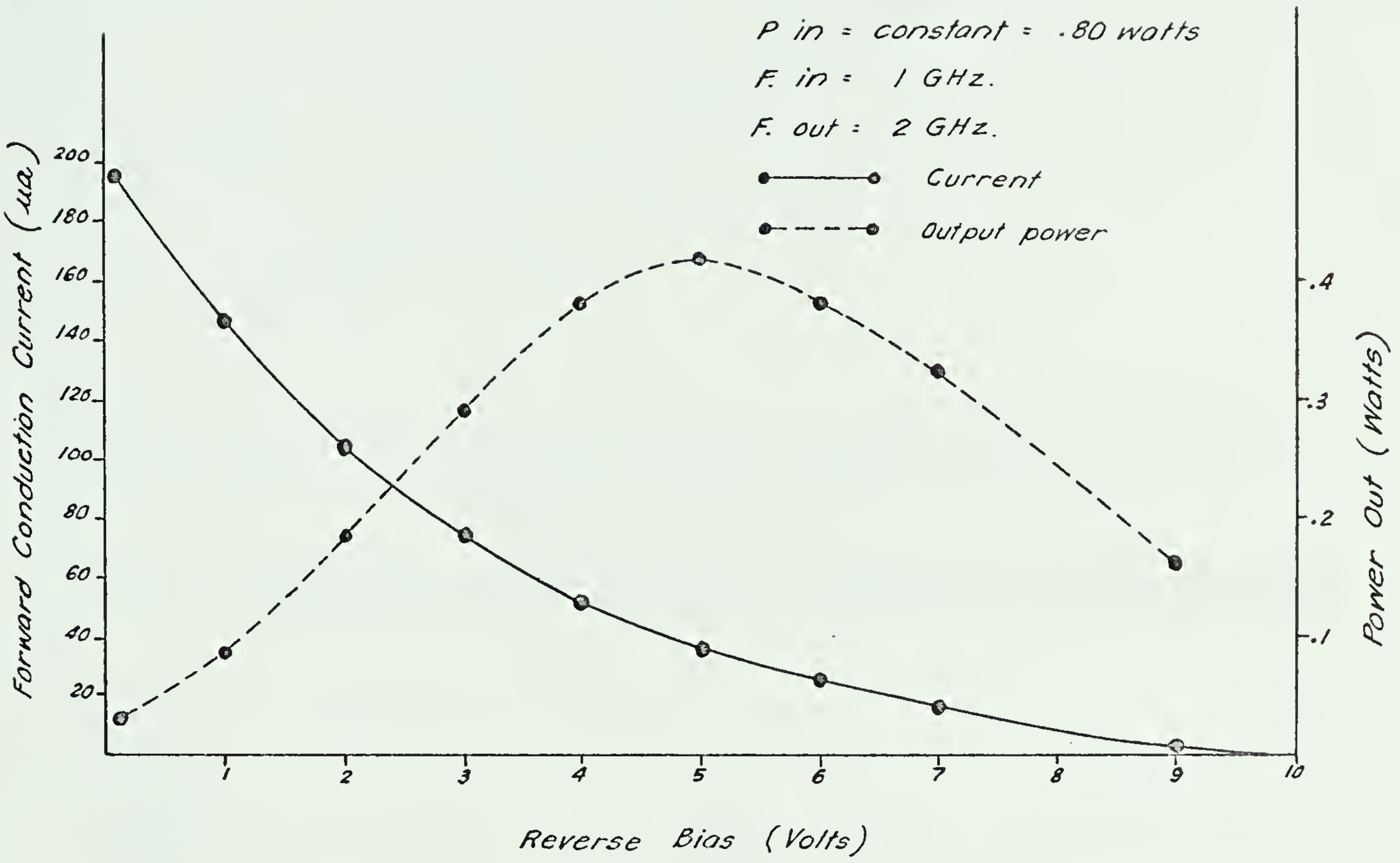
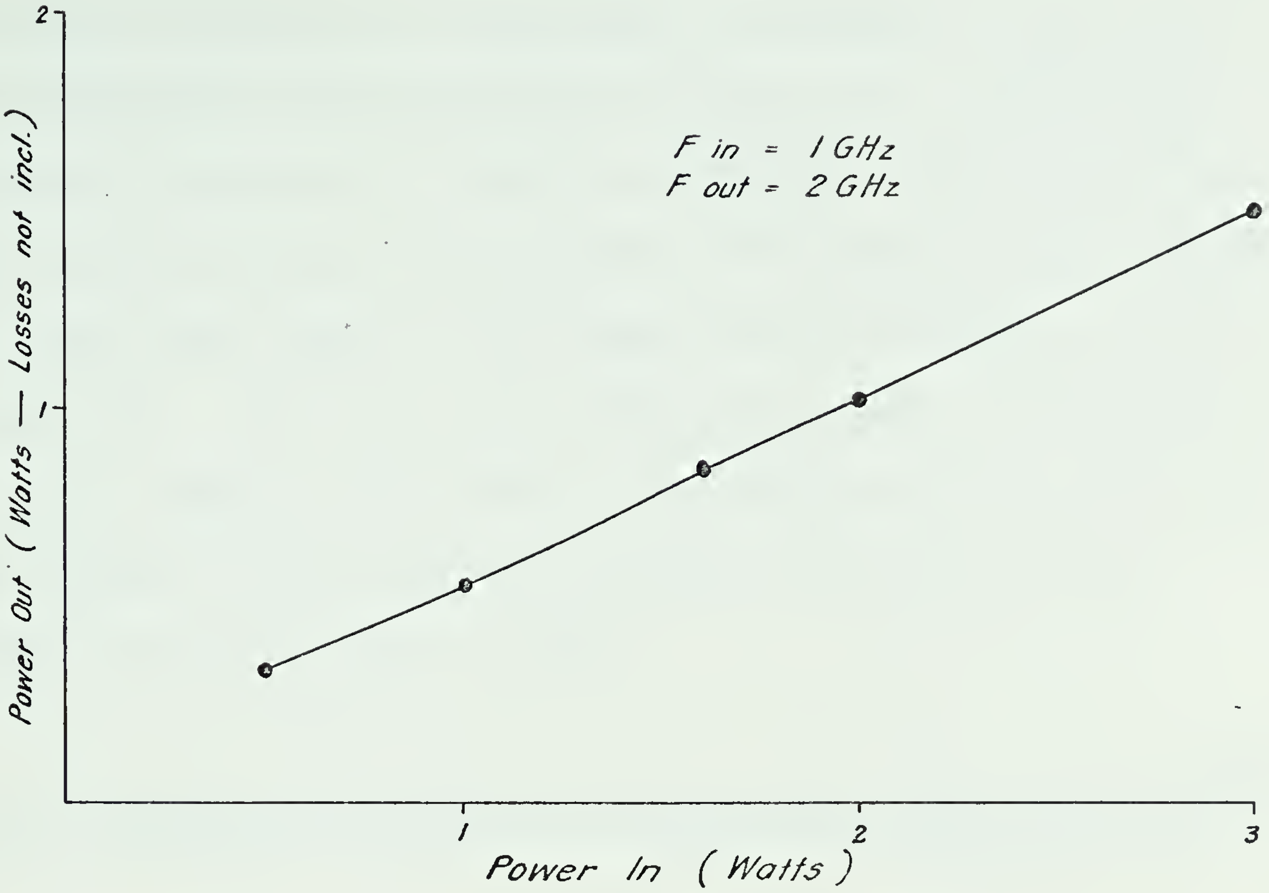
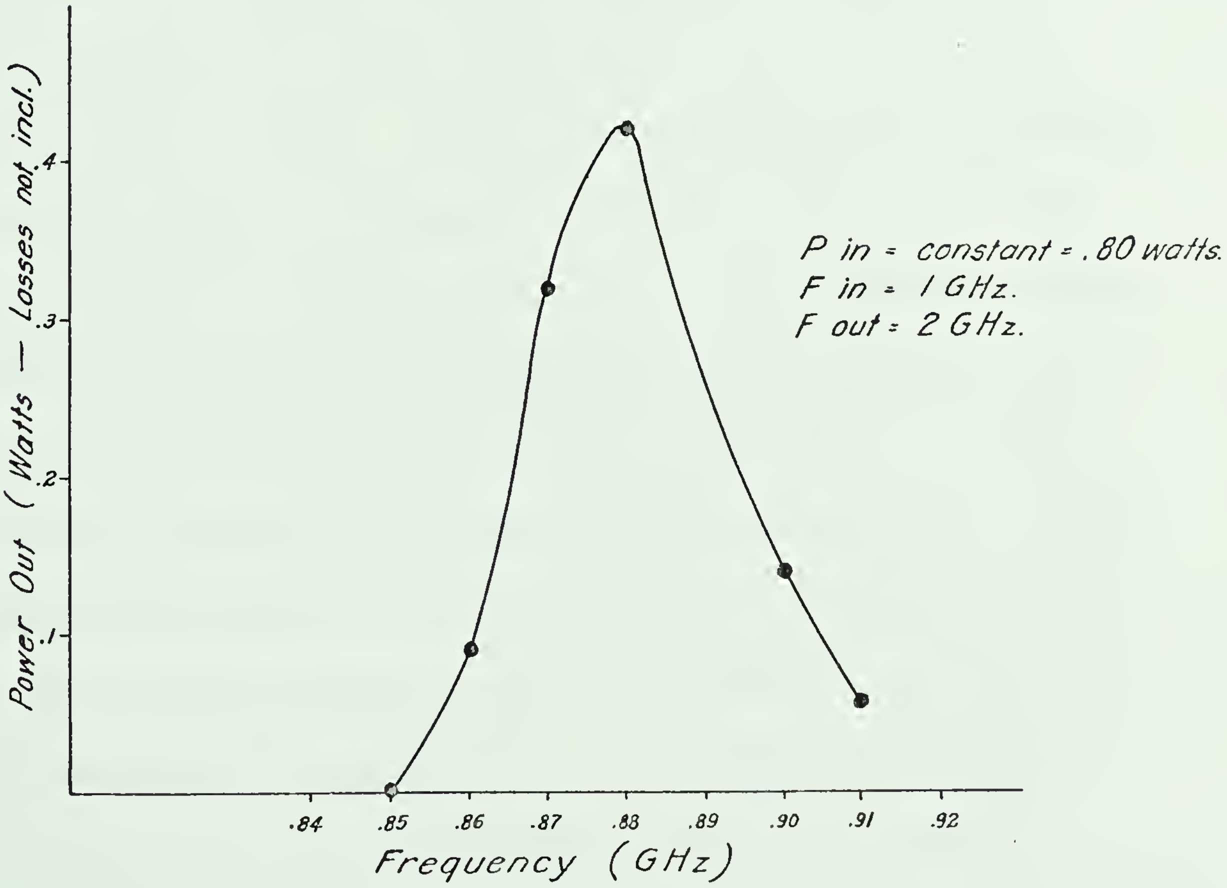


FIG. 4.4 REVERSE BIAS VS. FORWARD CONDUCTION CURRENT AND OUTPUT POWER (NO RETUNING)



F in = 1 GHz
F out = 2 GHz

FIG. 4.5 POWER IN VERSUS POWER OUT (BIAS VOLTAGE RETUNED)



P in = constant = .80 watts.
F in = 1 GHz.
F out = 2 GHz.

FIG. 4.6 POWER OUT VS FREQUENCY (NO RETUNING)

current and bias (no retuning) is plotted in Fig. 4.4, and bandwidth (no retuning) in Fig. 4.6. A 3db, non-retuned bandwidth of 2.4% was obtained. Theoretically, the bandwidth for the two-diode $\lambda/2$ spaced array, should be less than that of the single diode multiplier (2.5% obtained). However, since the Q was lower (54% efficiency as compared with 58% in the single-diode case) and the circuit containing the diodes was different, no valid comparison can be made.

4.2 Stripline Adaptation of Wilkinson Hybrid Circuit(25)

In order to examine power addition from several multipliers, a summing device having N isolated and matched output ports was necessary. Two of the more commonly used dividers, which can be adapted as summing devices, are shown in Figures 4.7A and 4.7B. In Fig. 4.7A, a corporate feed structure of T junctions provides the symmetry necessary to provide the equiphase, equi-amplitude condition independent of frequency. In Fig. 4.7B circular symmetry is employed where all the output terminals are connected to the common conductor of the coaxial line and combined load is matched by means of a quarter wavelength transformer. The first technique however gives poor isolation and requires a binary number of output ports whereas the second has the serious

disadvantage of no output isolation. The Wilkinson hybrid circuit however maintains phase and amplitude equality between any number of outputs independent of frequency, and in addition provides isolated and matched outputs.

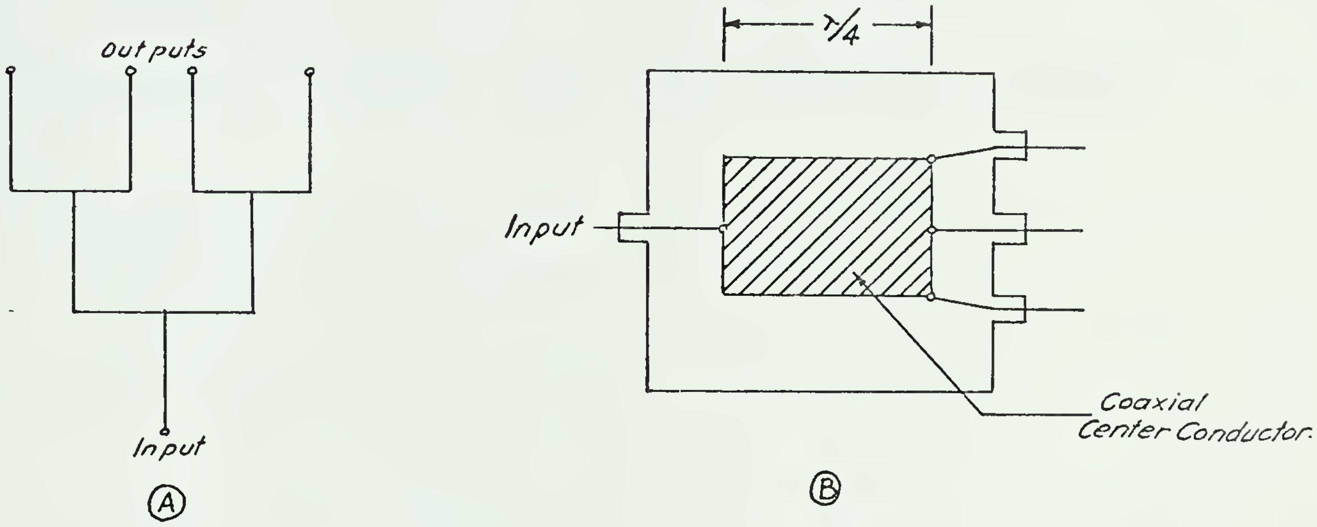


FIG. 4.7 Commonly Used Power Dividers

The power divider as proposed by Wilkinson is shown in Fig. 4.8. The circuit consists of a coaxial line in which the hollow inner conductor has been split into N splines of length $\lambda/4$. A shorting plate connects the splines at the input end and resistors connected in a radial manner between each spline at the output end and

a common junction. A reflected signal at any output power will travel partially via the resistors and the rest back to the input splitting again at the junction and returning to the output terminals. Thus the reflected wave arrives in two parts, one 180° out of phase with the other, when the splines are $\lambda/4$ in length. Proper choice of the resistive values and characteristic impedance of the spline transmission line ensures that the two parts of the reflected wave are of equal amplitude but opposite phase thus causing complete cancellation.

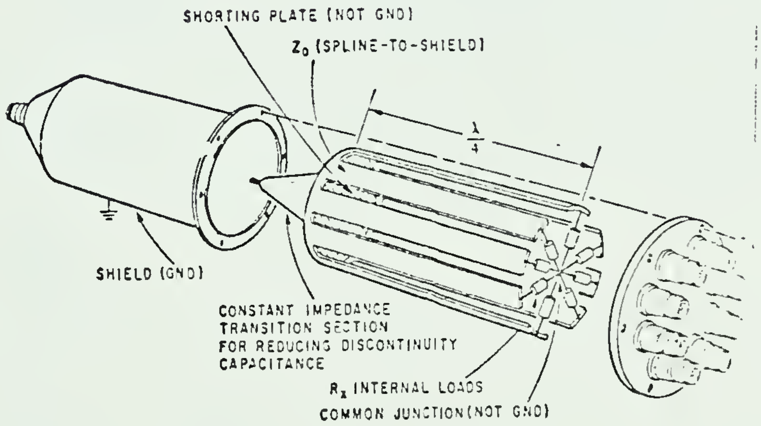

SHORTING PLATE (NOT GND)
Z_0 (SPLINE-TO-SHIELD)
$\frac{\lambda}{4}$
SHIELD (GND)
CONSTANT IMPEDANCE TRANSITION SECTION FOR REDUCING DISCONTINUITY CAPACITANCE
R_x INTERNAL LOADS
COMMON JUNCTION (NOT GND)

FIG. 4.8 Wilkinson Hybrid Circuit

All three devices discussed here can be utilized as power summing devices if input signals of equal phase and amplitude are applied at the output ports. Since isolation and input-output matching are required to sum power from several multipliers (in order to reduce tuning problems and maintain efficiency respectively) the Wilkinson device was chosen. However, stripline rather than co-axial cable was utilized. The proposed two port, stripline adaptation of the divider is shown in Fig. 4.9 and its equivalent circuit in Fig. 4.10. Applying the transmission line equations and using the notation of Fig. 4.10:

$$V_1 = V_a\cos\theta + jI_{1a}^{1}Z_0\sin\theta = jI_{1a}Z_0 \tag{4.5}$$

$$I_{1a} = j\frac{V_a}{Z_0} \tag{4.6}$$

$$V_a = jI_{a2}Z_0 \tag{4.7}$$

$$I_{2a}^{\;1} = j\frac{V_2}{Z_0} \tag{4.8}$$

$$I_{1a}^{\;1} = V_a/R_0 + I_{2a}^{\;1} \tag{4.9}$$

$$I_{2a} = V_2/R_0 - I_{1b} \tag{4.10}$$

$$(I_{1b} + I_{1a})R_0 = V - V_1 \tag{4.11}$$

$$(I_{1b} + I_{2b})R_x = V_1 - V_2 \tag{4.12}$$

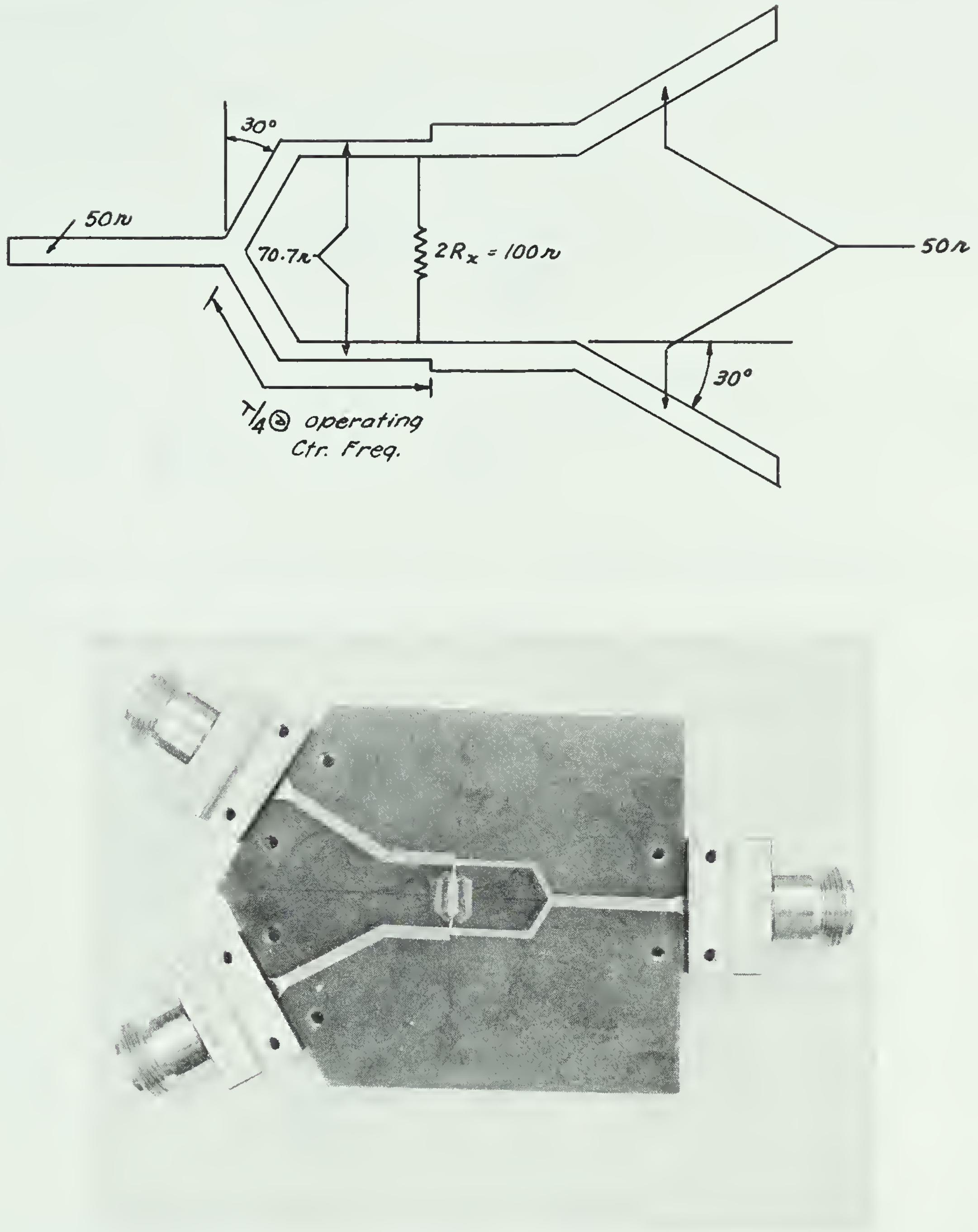


Fig. 4.9 Stripline adaptation of Wilkinson Hybrid Circuit

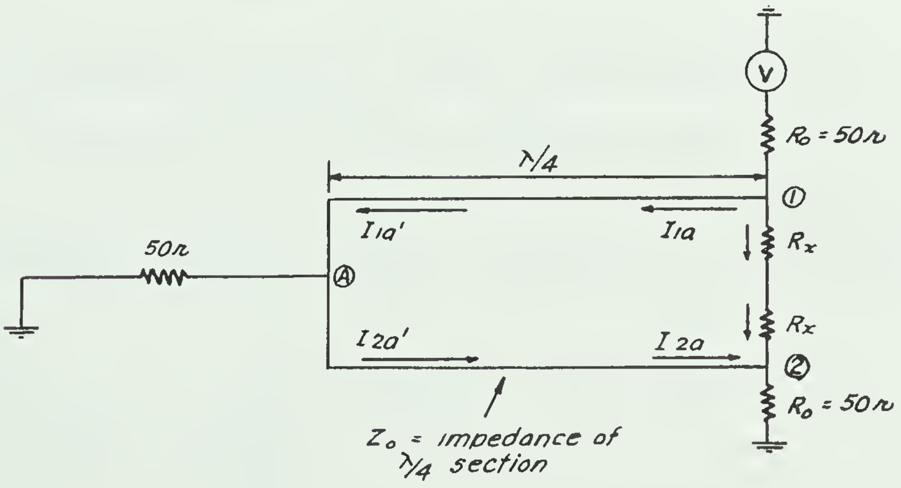


Fig. 4.10 Equivalent circuit for Fig. 4.9

Equations (4.5 - 4.8) and (4.9 - 4.12) may be combined to show that

$$V_a + jR_{0/Z_0}V_2 + jV_{1/Z_0} = 0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4.13)$$

$$jV_aR_0/Z_0 + (1 + R_{0/2R_x})V_2 - \frac{V_1R_0}{2R_x} = 0 \quad \ldots\ldots\ldots\ldots(4.14)$$

$$jV_a\frac{R_0}{Z_0} - \frac{1}{2}\frac{R_0}{R_x}V_2 + V_1(1 + \frac{R_0}{R_x}) = V \quad \ldots\ldots\ldots\ldots\ldots(4.15)$$

For perfect isolation $V_2 = 0$, and the equations 4.13 to 4.15 may be combined to yield

$$\frac{V_1}{V} = \frac{1}{1 + R_{0/R_x}} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(4.16)$$

or

$$\left(\frac{R_0}{Z_0}\right)^2 = \frac{R_0}{2R_x}$$

and for matched output admittances, one obtains

$$Y_1 = \frac{I_{1b} + I_{1a}}{V_1} = \frac{V - V_1}{R_0V_1} = \frac{1}{R_0} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots(4.17)$$

Combining (4.10) and (4.11) yields

$$R_x = R_0$$

$$Z_0 = 2R_0$$

The input impedance under these conditions will be the parallel combintation of two output loads R_0, after each has been transformed through a quarter wavelength of line Z_0. Hence

$$Z_{input} = \frac{Z_0^2}{R_{0/2}} = R_0 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots(4.18)$$

The proposed divider (Fig. 4.9) was designed to have a center frequency of 2GHz but was found experimentally to be 1.85GHz. In the theoretical model, the resistor $2R_x$ was assumed to have negligible length, whereas in the circuit constructed it was of the order of $.12\lambda$.

The principal effect of this appears to be that it shifts the center frequency for best performance to a lower value than design frequency, and perhaps, change the effective resistance of the internal loads, since the current through the length of the resistor may not be uniform. Isolation and output V.S.W.R. values were obtained using a 100Ω. $\frac{1}{4}$ watt composition resistor for the two 50Ω internal loads. The measured isolation characteristics are plotted over the frequency range 1.2GHz in Fig. 4.11. The output and input V.S.W.R.'s are plotted in Fig. 4.12.

4.3 Two Diode Doubler Utilizing Wilkinson Hybrid Circuit

To this author's knowledge, all high power multipliers constructed to date, with the exception of Bartnik's(26), contains N diodes arranged in one or a combination of the array types discussed in the introduction. Power summation of separate multipliers seems to have been ignored as increased circuitry, and therefore cost, is

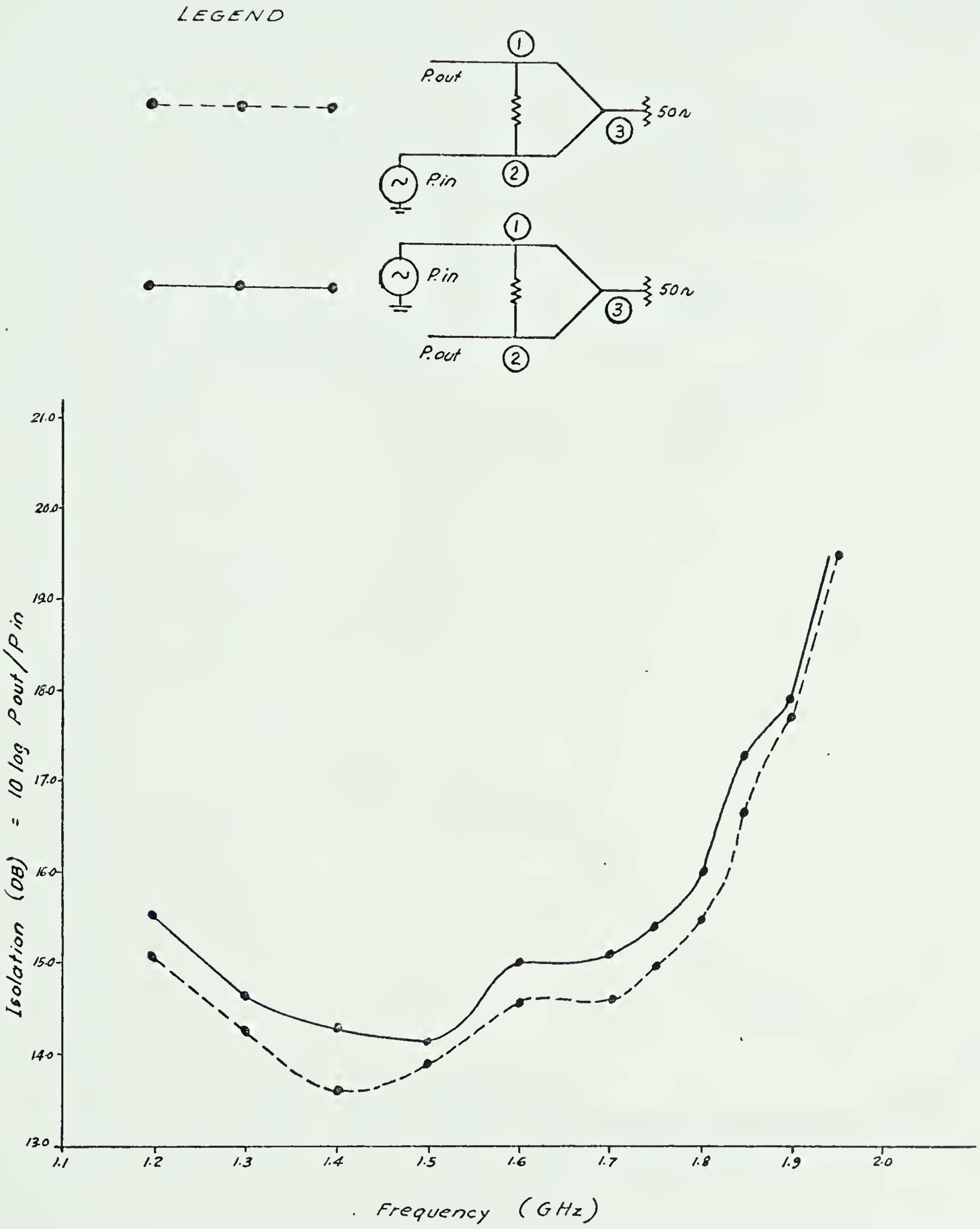


FIG. 4.11 ISOLATION OF POWER DIVIDER VS FREQUENCY

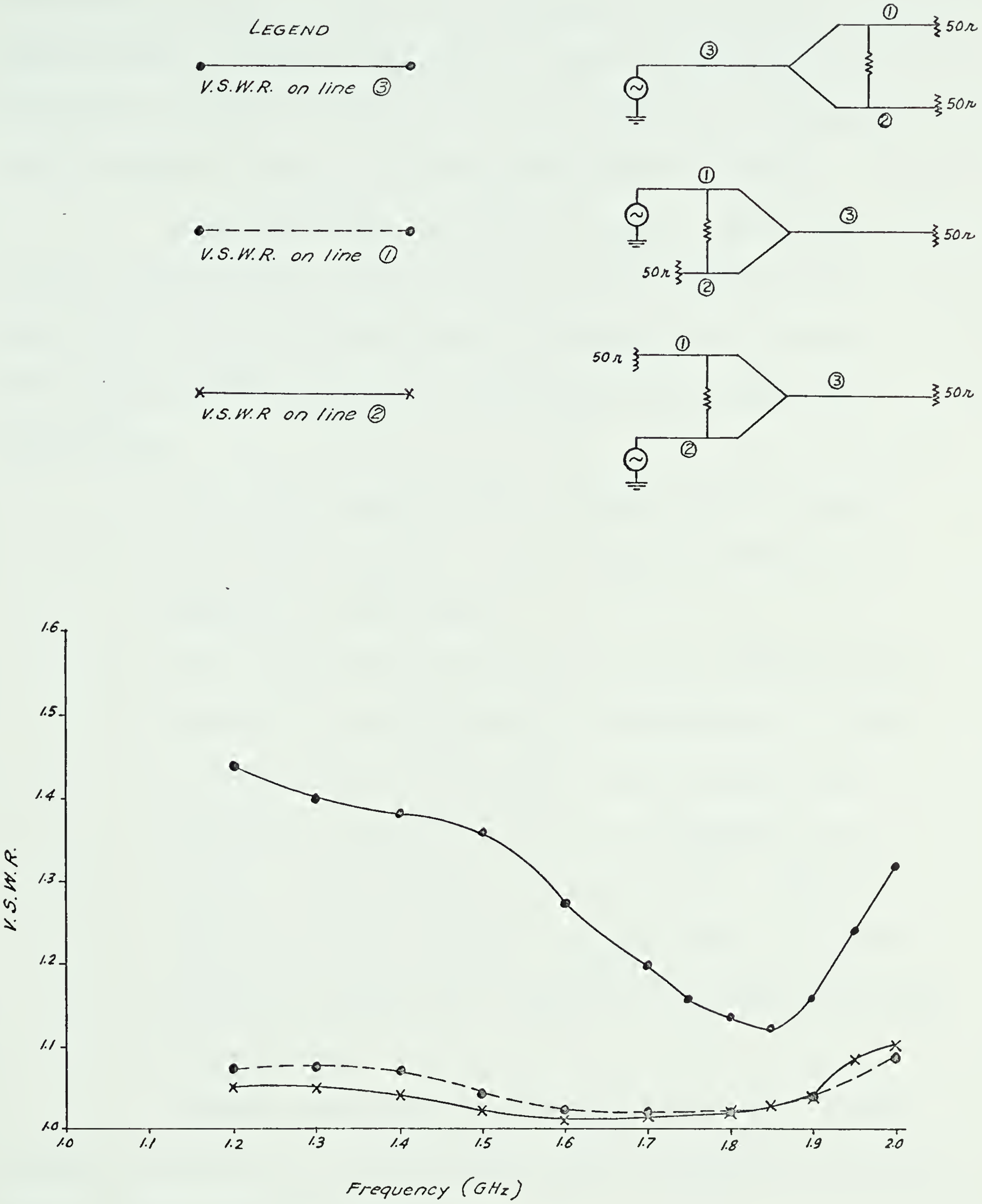


FIG. 4.12 INPUT AND OUTPUT V.S.W.R.'s VS FREQUENCY

involved. Thus, in the investigation of harmonic generators of the second type, it was of interest to simplify component design (filters, matching devices, etc.) without degrading efficiency and isolation.

The two-diode stripline doubler tested is shown in Fig. 4.16. Input matching and equal power distribution are accomplished by means of a co-axial "T" junction(27), when the following conditions are satisfied:

(1) The inherent "T" junction susceptance is small compared to the characteristic impedance of the line.

(2) The diode impedances at the driving frequency (Z_1 and Z_2 resp.), transformed to the T junction (Z_1^1 and Z_2^1), must combine to yield Z_0, the characteristic impedance required to match the input section. This is possible when $/K_1\underline{\angle\theta}/ = /K_2\underline{\angle\phi}/$ where K is the voltage reflection coefficient associated with Z_1 and Z_2.

If the junction susceptance is large, tuning screws inserted at the junction can be adjusted to resonate at the input frequency.

Filtering was accomplished by means of single stubs (Fig. 3.3) and output matching by double stub tuners. A trombone phase shifter was inserted into output arm (2),

ensuring equi-phase signals to the Wilkinson hybrid circuit.

The effect of bias change on output power is shown in Fig. 4.17. Output power versus input power and frequency are plotted in Figures 4.18 and 4.19 respectively.

The coaxial "T" junction, when matched or nearly so, could be considered to be a center fed, magnetically coupled cavity terminated at each end in low impedance. As frequency increases, these terminations better approximate a lossy short. In the circuit tested, the output frequency (1.85GHz) is, to a first approximation, isolated from the input by the $\lambda/8$ stub. However, higher even harmonics are not affected, while the odd see an additional susceptance of magnitude G_0 at the stub intersection. Since the distance separating the diodes is some multiple $N(N = 1,2, \ldots.)$ of $\lambda/2$ at the input frequency, higher order harmonics can flow, as is the case with the $\lambda/2$, two diode type array. However, the two diode phase shift array requires an input matching device which is accomplished in the test circuit by the coaxial "T". Thus, for input matching, the conventional phase shift array has no advantage with respect to the amount of circuitry involved.

In order to match the "T" junction, assuming its inherent susceptance is negligible or has been tuned out, it was necessary that $/K_1\ \theta/ = /K_2\ \phi/$ where K is

the voltage reflection coefficient associated with the diodes. For small, normalized diode impedances, $/K_1\underline{/\theta}/$ $/K_2\underline{/\phi}/$ when $R_1 = R_2$. This is of significant interest as matching can be accomplished when, for certain ranges, the reactive components of the diodes are not equal (with equal power distribution). In a conventional array, it is essential that matched diodes are utilized as reactive mismatch introduces unequal input power distribution and output phase which both tend to decrease desirable output power and introduce additional odd harmonics.

Tuning proved to be relatively simple if the following procedure was followed:

(1) Having set the bias elements adjust line stretchers (1) and (2) (Fig. 4.16) such that equal power distribution and matching occurs. This can be determined by utilizing directional couplers or the method proposed in Section 3.3.

(2) Adjust the trombone phase shifter for equiphase output [least losses occur in the power divider for equiphase, equiamplitude inputs] followed by tuning of the double stub tuners for maximum output signal.

Since the filtering system utilized does not provide complete input-output isolation this procedure

may have to be repeated. Unlike conventional systems which utilize standard filters, output isolation of the fundamental (35db) is accomplished in this system by the double stub tuners and the power divider.

An interesting feature of the circuit was that when line stretchers (1) and (2) were adjusted for equal power distribution ($P_{INC(1)} - P_{ref(1)} = P_{INC(2)} - P_{ref(2)}$) and matching ($P_{ref} = 0$), P_{IN} was less than the sum of $P_{IN(1)}$ and $P_{IN(2)}$ by approximately 6 db (Fig. 4.16). However, the total transmitted power ($P_{INC(1)} - P_{ref(1)} + P_{INC(2)} - P_{ref(2)}$) was equal to the input power when circuit losses were accounted for. This effective "increase" in incident power can be explained utilizing experimental results obtained with the circuit shown in Fig. 4.13.

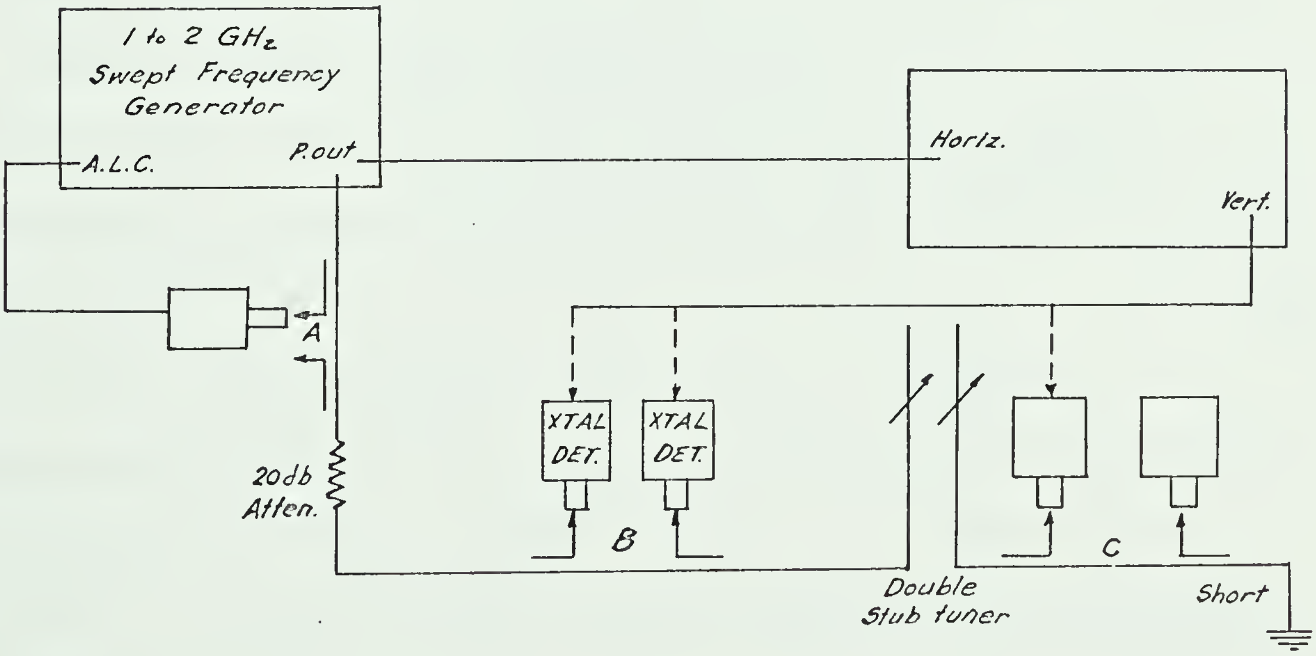
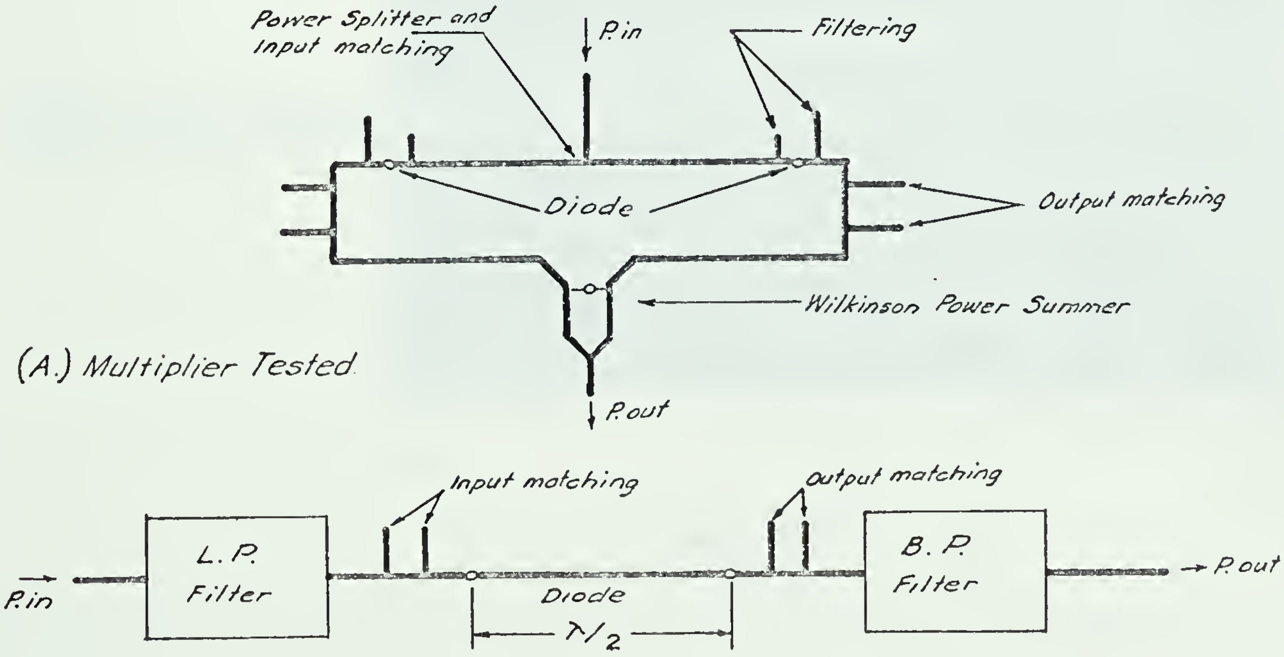


FIG. 4.13 Circuitry Utilized To Show Cavity Effect

Three 20db directional couplers (H.P. coaxial 940.19001·1Hz) were used, (A) for level control, (B) to measure incident and reflected power and (C) to measure transmitted power through the stubs. Monitoring the signal at these points did not seriously affect the wave pattern in the main line as coupling was weak (20db). The 20db attenuator was inserted to ensure constant output power fromthe source ($P_{INC(B)}$ = constant). By adjusting the double stub tuner it was possible to make $P_{INC(C)} > P_{INC(B)}$ for particular frequencies, indicating that the line section to the right of the double stub tuners becomes a low Q, coaxial cavity. At these frequencies, power is being transmitted to the coupler ($P_{ref(B)} \ll P_{INC(B)}$). However reflected power from the short terminating C is once again reflected at the tuning stub such that constructive interference occurs. Photographs shown in Fig. 4.14 show the effect of various tuning stub configurations. This "cavity" effect would seem to be the reason for the apparent increase in incident power. As the diode impedances terminating the input circuit are small compared to the characteristic line impedance and their separation is approximately $N\lambda/2$, (N = 1,2, ...) at the driving frequency, Fo, the input circuit forms, to a rough approximations, a coaxial cavity, thus explaining the increase in power levels.

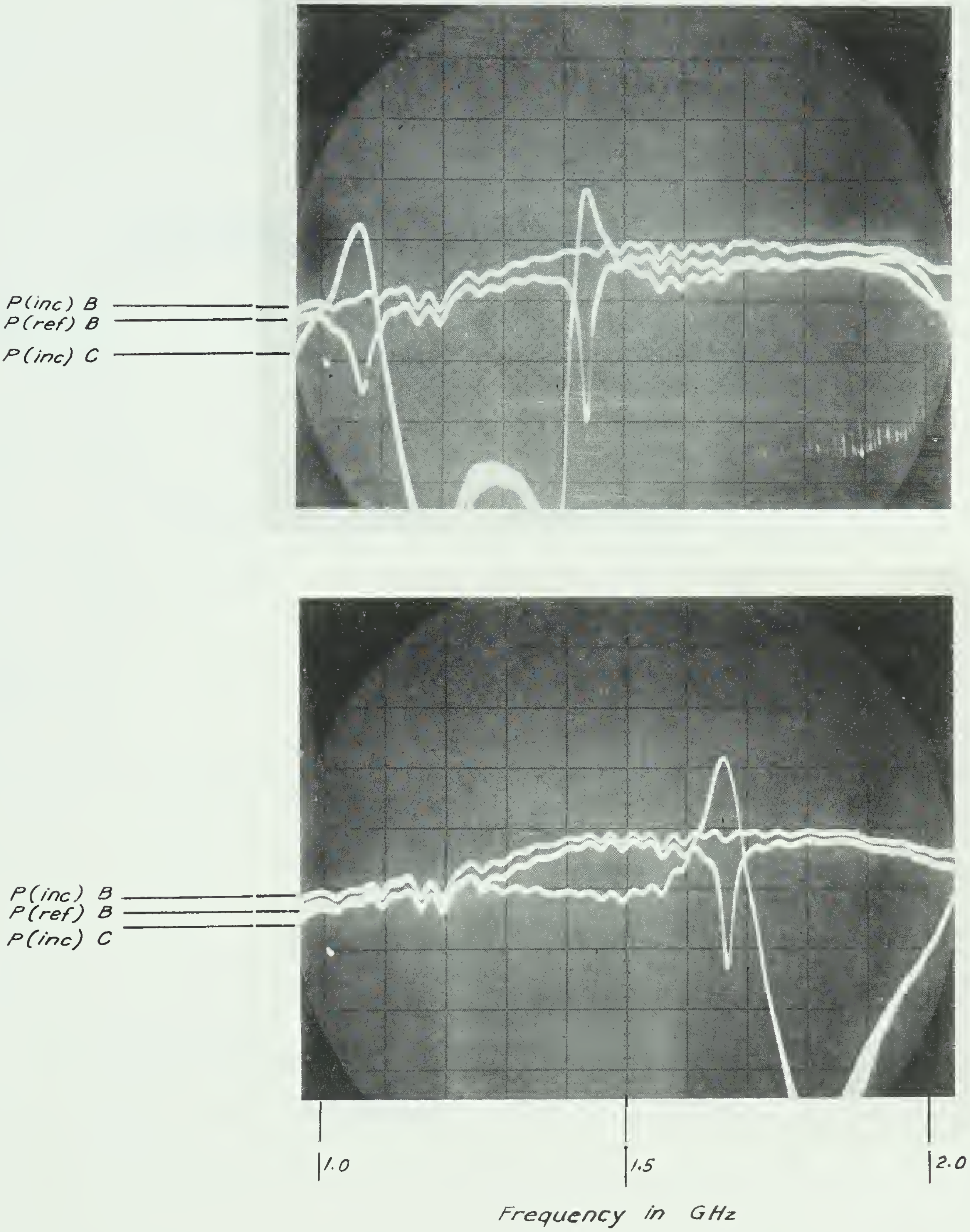
In summary the doubler tested compared favourably (60% efficiency) to results obtained using conventional methods. The circuitry required was no greater than that of conventional methods and the design is perhaps simpler. A stripline adaption of the multiplier tested and that required for a 2-diode, phase-shift-type array of comparable performance is shown in Fig. 4.13, indicating the required circuitry involved for each. Heat sinking and reliability would seem to be adequate. If a stripline power-summer employing ferrite substrates could be utilized, this type of system could more readily be designed to provide greater output power in the event of a single diode failure as only input matching would be affected, as compared to a phase shift array where input and output matching would be disrupted.



(A.) Multiplier Tested

(B.) $\lambda/2$ Phase Shift Array

FIG. 4.14 Stripline Adaption (Top View of Center Conductor) For The Hybrid Doubler



Vertical Scale : 5db = 1 Division (Power)

FIG. 4.15 DIRECTIONAL COUPLER CAVITY EFFECT

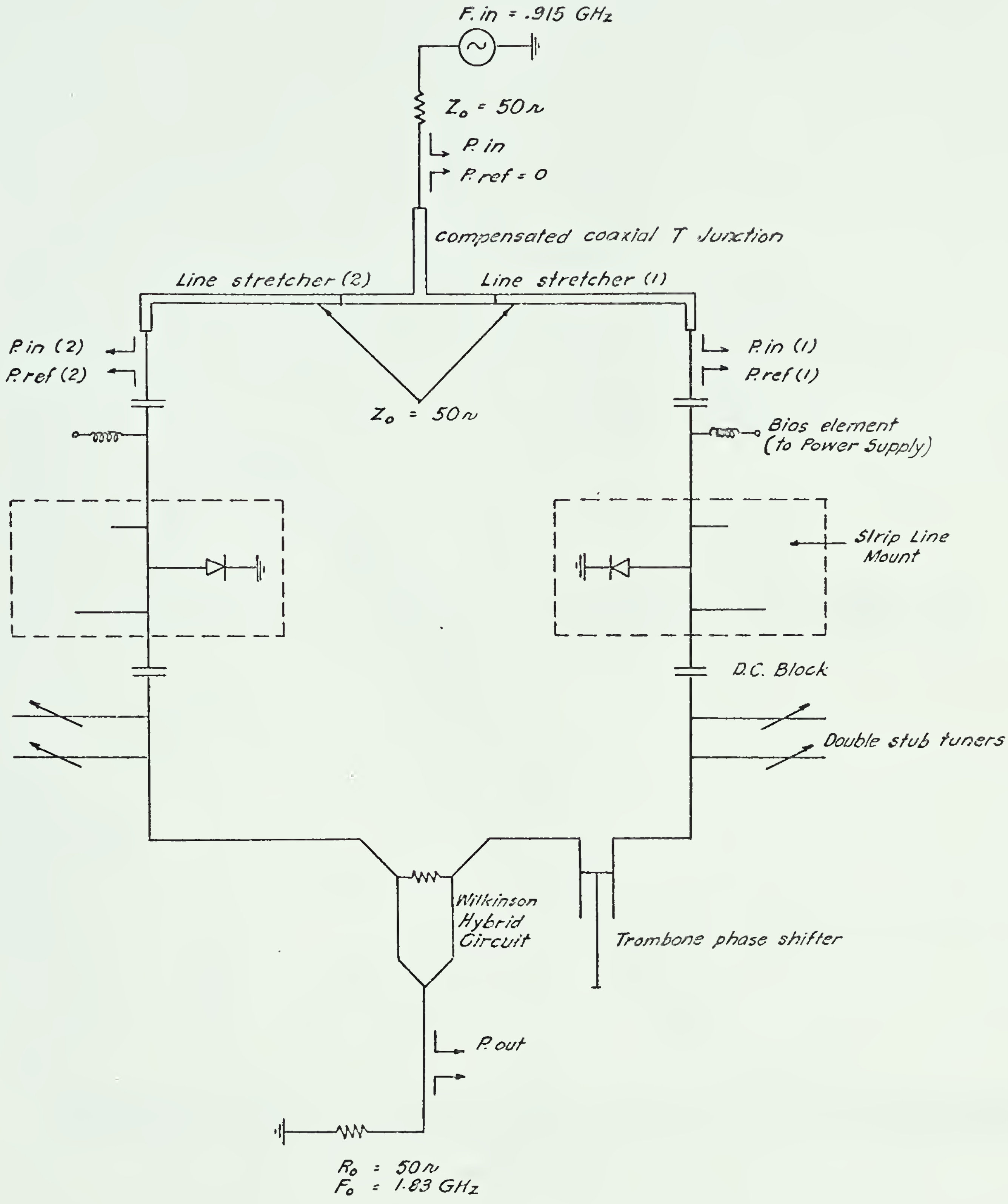


FIG. 4.16 TWO DIODE DOUBLER UTILIZING WILKINSON HYBRID CIRCUIT.

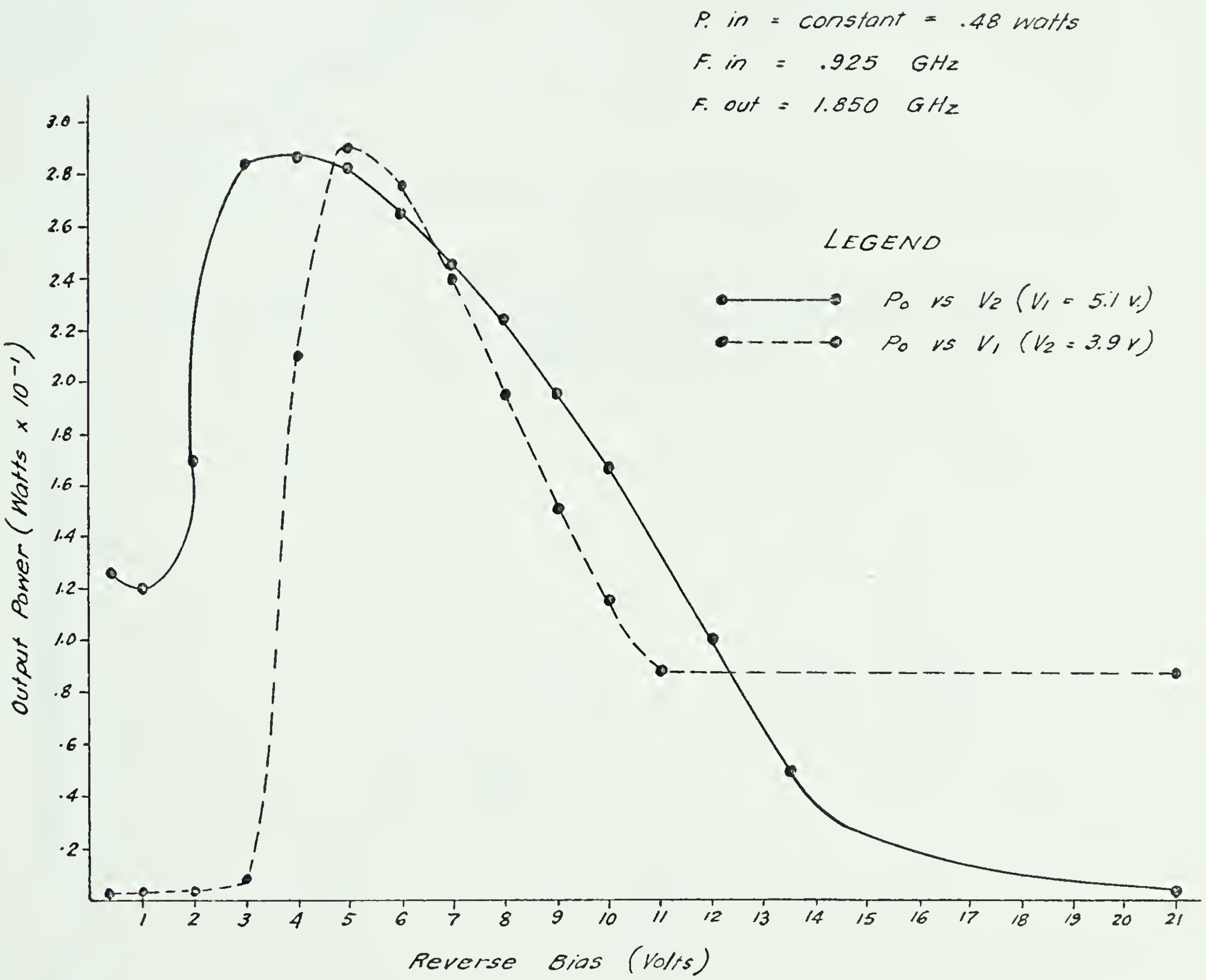


FIG. 4.17 OUTPUT POWER VERSUS BIAS (NO RETUNING) FOR THE HYBRID DOUBLER.

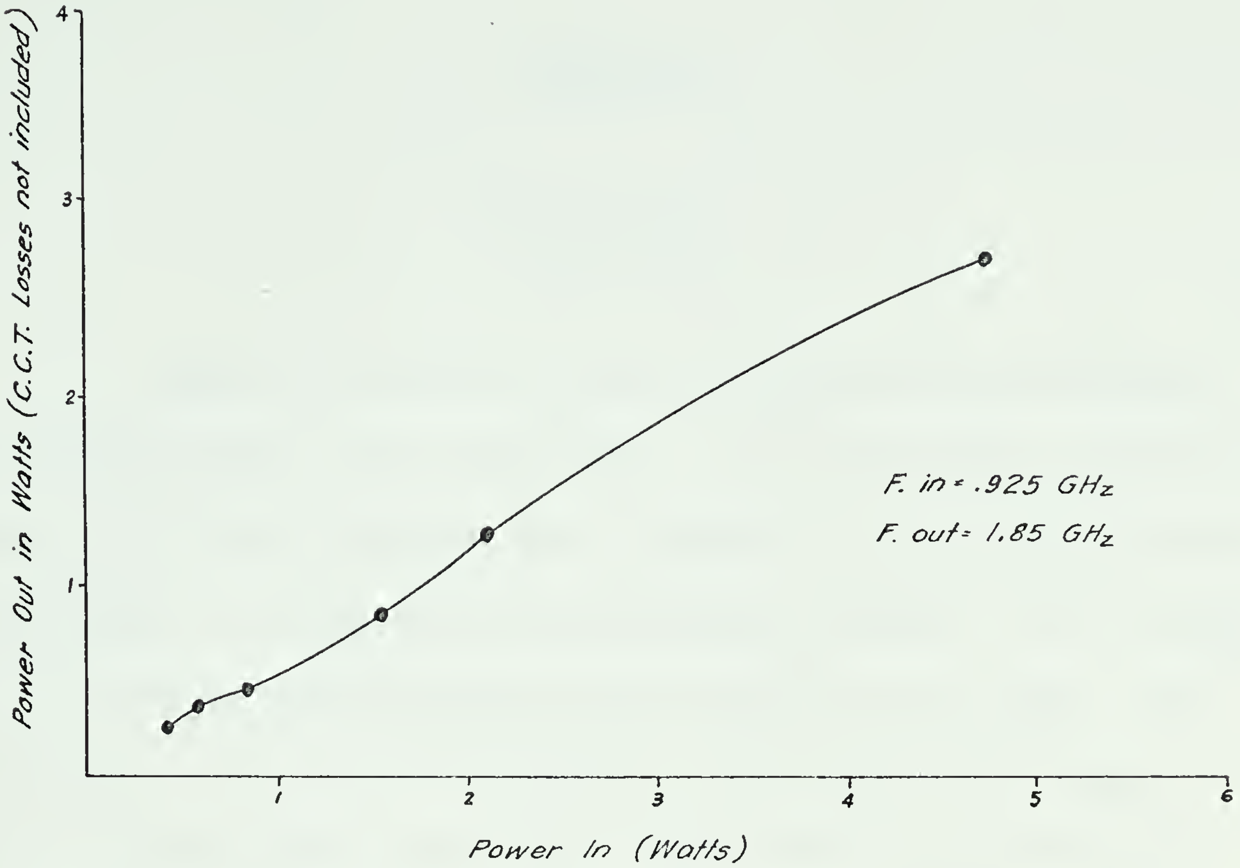


FIG. 4.18 POWER OUT VS POWER IN (BIAS VOLTAGE RETUNED) FOR THE HYBRID DOUBLER.

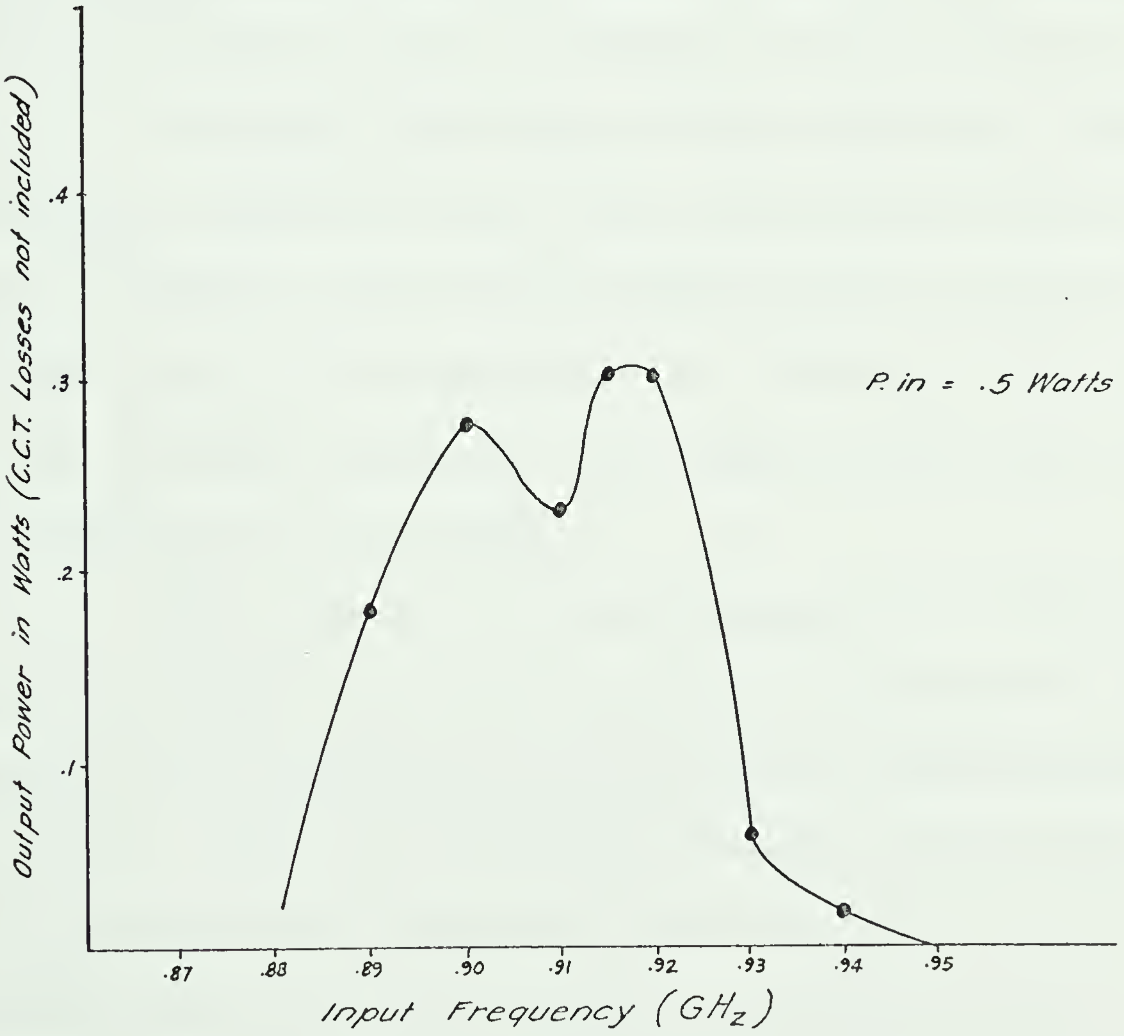


FIG. 4.19 OUTPUT POWER VS FREQUENCY (NO RETUNING) FOR THE HYBRID DOUBLER.

CHAPTER V

Conclusion

Some aspects of step recovery diode harmonic generators have been examined. A set of design equations (Sect. 3.5) was derived for a doubler utilizing quarter wavelength transformers as matching devices. The analysis, although dealing with the single diode case, can readily be adapted to a N-diode chain as arbritrary diode impedance was assumed. The effect of incident power and harmonic generation efficiency on recombination current in such a multiplier was presented.

A method for tuning an N-diode chain, where the diodes operate in the step recovery mode, was proposed, allowing one to tune power multipliers which utilize arrays with greater ease. Economy, with respect to the necessary equipment and experimental ease were two features of the method.

The problem of diode mismatch and its effect on conventional multi-diode arrays with respect to performance was examined theoretically and experimentally. A harmonic generator essentially consisting of two multipliers with a Wilkinson hybrid circuit to sum their outputs was shown to be capable of satisfactory operation when mismatched diodes were employed. The

circuitry required was no greater as compared to conventional multi-diode arrays, the performance was comparable, and the design perhaps simpler.

Several possible areas for future study would seem apparent. It would be desirable to investigate recombination current in the step recovery diode as a function of frequency and incident power. With proper refinements and experimental data it would seem possible to predict diode impedance when the source power and frequency were known from the magnitude and direction of the D.C. bias current. It would also be of interest to examine multi-diode harmonic generators which utilize a ferrite device to sum output power from separate multipliers. Thus, isolation between output ports would be maintained in the event of failure of one or several multipliers. If a power divider was used at the input, P.I.N. switching diodes, sensitive to bias current, could be incorporated in the circuit such that mismatch, and thus loss of available input power did not occur in the event of such failure. For example, if a particular diode failed, the bias current would cease, and the P.I.N. diode, sensitive to bias current, would be driven into forward conduction, essentially becoming a "short". With the proper choice of geometry, this "short" would transform to the input power divider such that mismatch, and thus loss of

available input power did not occur. This type of circuit would have the advantage of greater reliability.

APPENDIX I

Lowpass Filter Design

A filter structure of the type shown in Fig. AI.1 (ie. infinite attenuation at finite frequencies) was considered as a sharp cutoff rate was obtainable (28). Fig. AI.2 illustrates the fashion in which the filter depicted in Fig. AI.1 can be approximately constructed in printed circuit stripline. The various elements are seen to be approximated by the use of short lengths of high and low impedance lines(29). The T.E.M. equivalent circuits shown in Fig. AI.3 were used to calculate the necessary dimensions, with additional susceptance or reactance associated with the π or T section respectively being compensated for. As an example, at the junction of the inductive line elements for L_1, L_2 and L_3 in Fig. AI.2, a total undesirable capacitive susceptance of $w_1 C_L = w_1(C\ )_1 + w_1(C\ )_2 + w_1(C\ )_3$ exists, due to the three inductive line elements. The susceptance $w_1 C_L$ can be compensated for by correcting the susceptance of the shunt branch formed by L_2 and C_2 so that

$$B_2 = w_1 C_L + B_2^C$$

where B_2 is the susceptance at frequency w_1 at the branch formed by L_2 and C_2 in Fig. A2.1, and B_2^C is the suscep-

tance of a "compensated" shunt branch which has L_2 and C_2 altered to become L_2^C and C_2^C in order to compensate for the presence of C_L. Fringing capacitance (edge effects) was also compensated for, however corner fringing was not as no satisfactory data was available.

The filter was designed to have an input-output impedance of 50Ω, 51 db out-of-passband attenuation and a cutoff frequency of 1.1GHz(w_1). The following normalized (to 50r) values(27) satisfied these requirements.

$w_1L_1' = .9439$

$w_1L_2' = .2298$

$w_1C_2' = 1.242$

$w_1L_3' = 1.399$

$w_1L_4' = .4078$

$w_1C_4' = 1.211$

$w_1L_5' = 1.256$

$w_1C_6' = 1.146$

A photograph of the completed structure with the upper section of the stripline assembly is shown in Fig. AI.4. Circuit dimensions and frequency characteristics are shown in Fig. AI.5 and AI.6 respectively. Tuning screws were inserted at the locations indicated in Fig. AI.3 to reduce the input-output V.S.W.R.

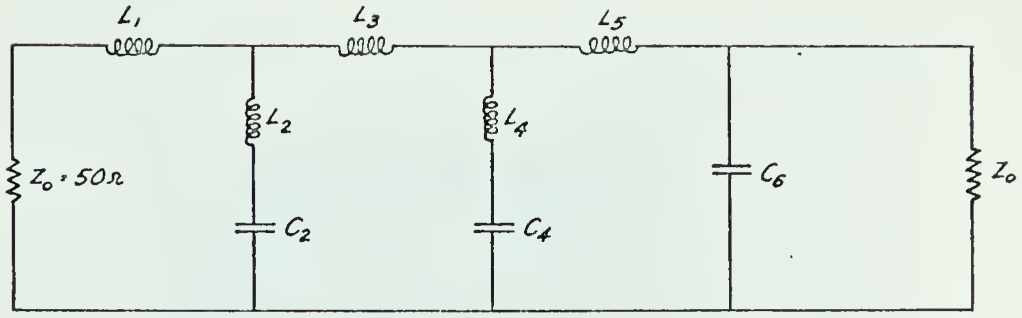


FIG. AI.1 Lowpass Filter Prototype

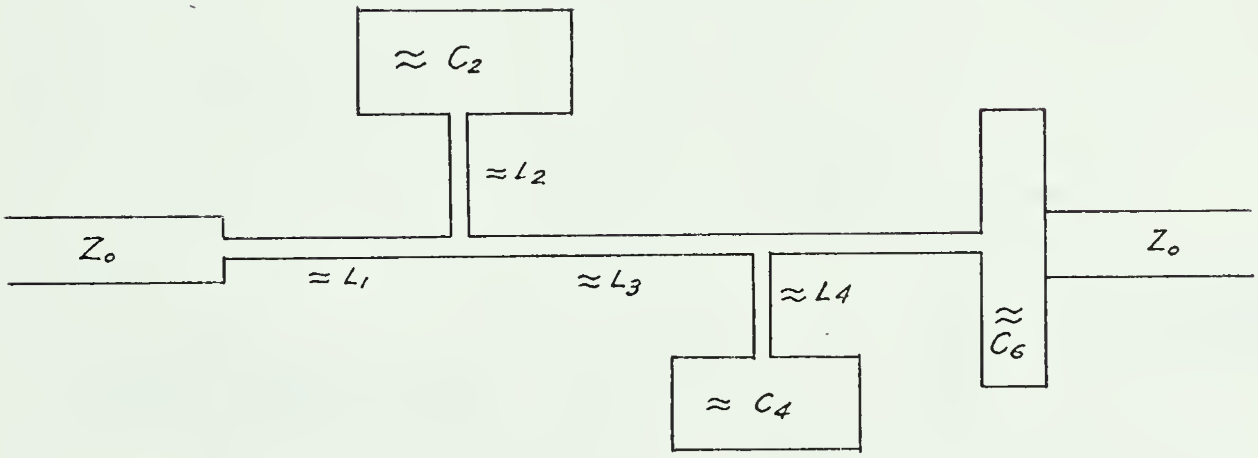


FIG. AI.2 Stripline Realization Of Fig. AI.1

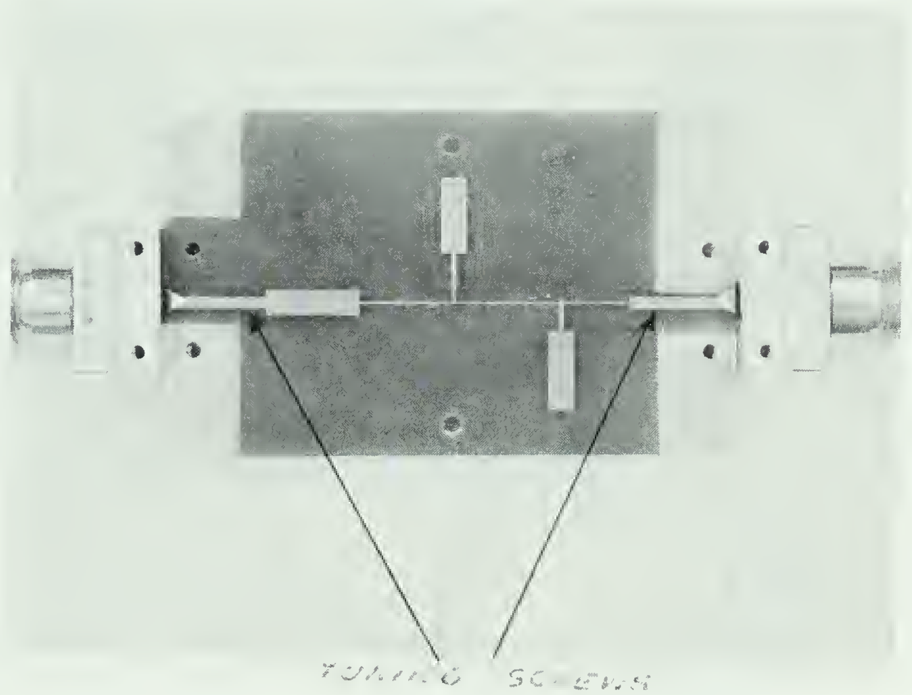


FIG. A 1.3 PHOTOGRAPH OF L. P. FILTER

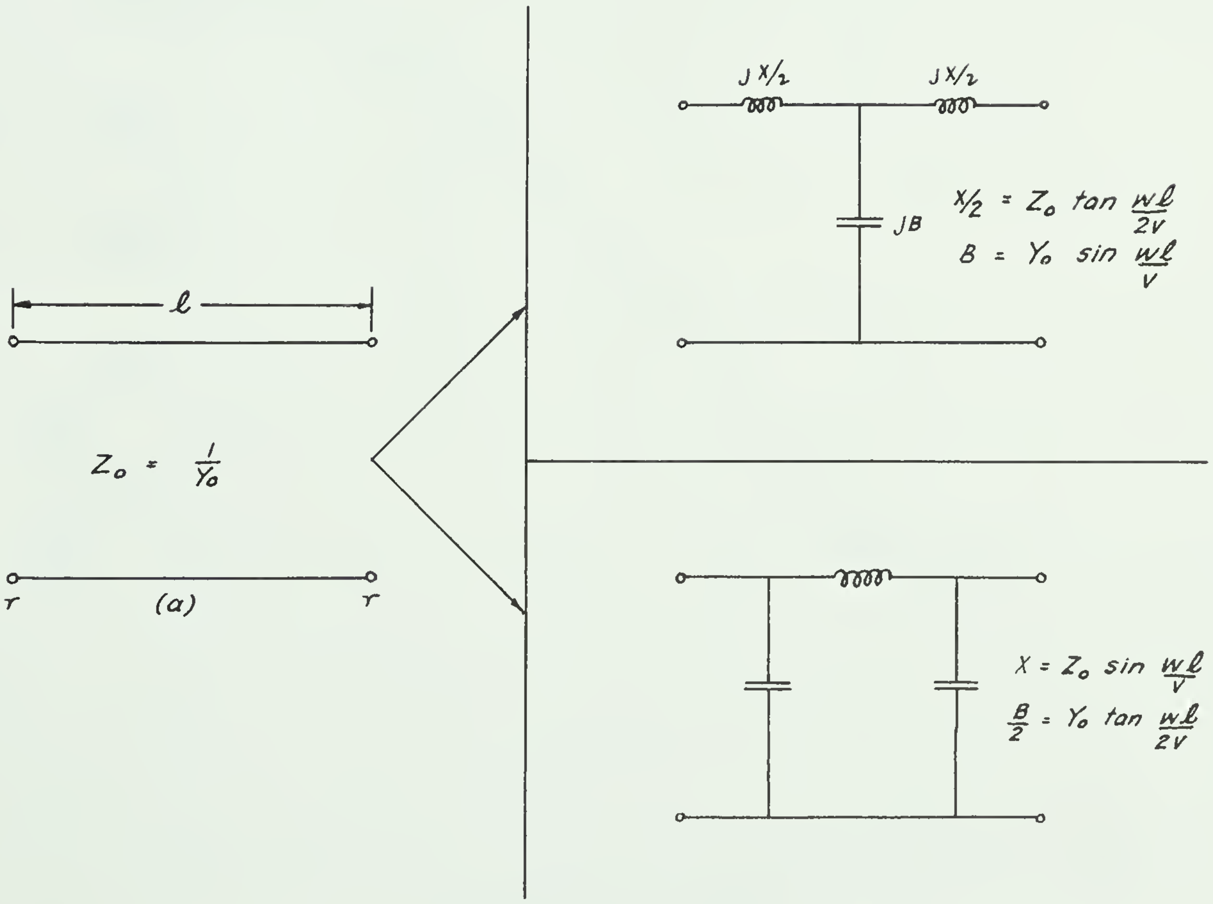


FIG. A 1.4 T.E.M. LINE EQUIVALENT CIRCUITS

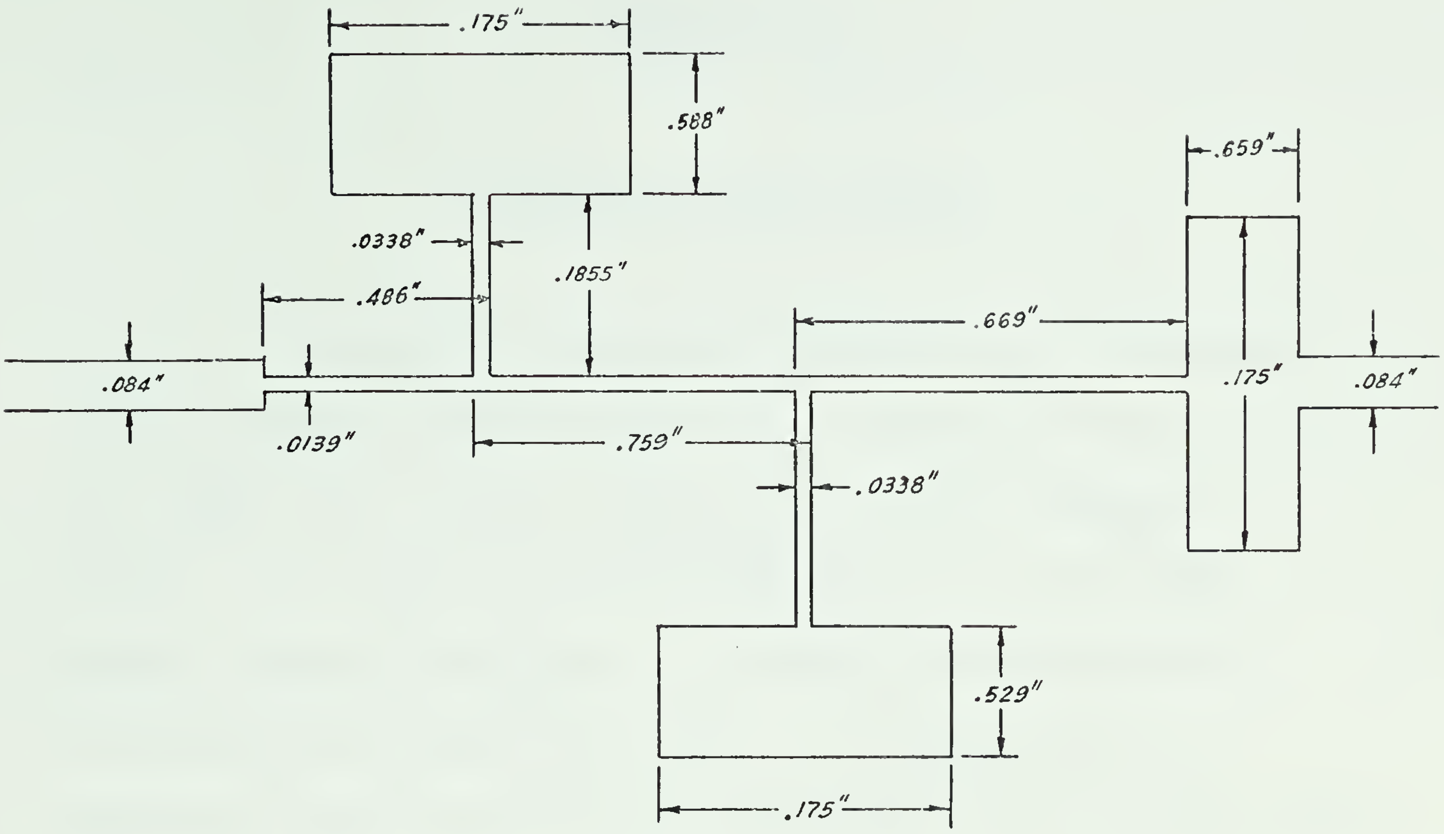


FIG. A1.5 CIRCUIT DIMENSIONS

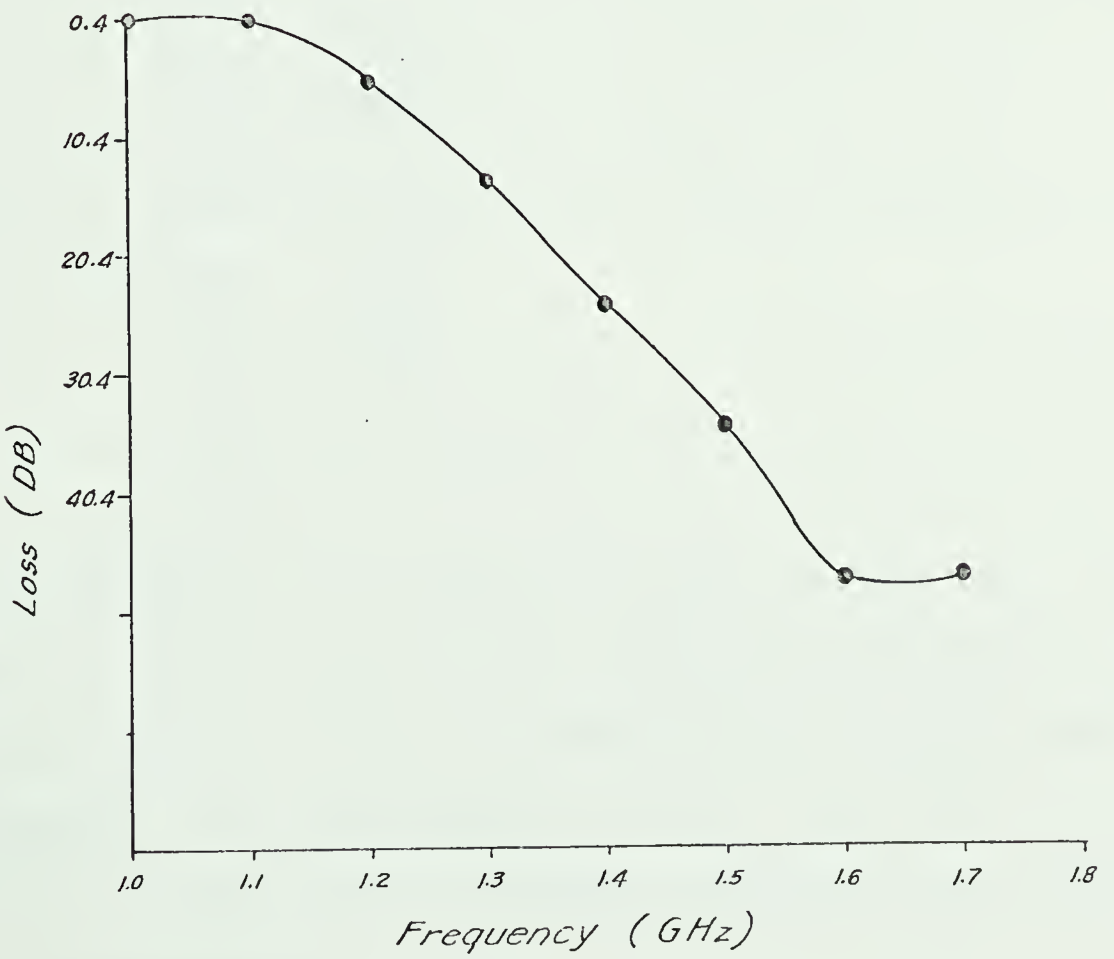


FIG. A1.6 LOW PASS FILTER FREQUENCY RESPONSE

APPENDIX II

Highpass Filter Design

Using the Tchebysheff prototype, a bandpass filter was designed to have the following characteristics - w_0 = 2GHz (ctr. freq), bandwidth = 10%, bandpass ripple = .01 db, and 38 db attenuation at 1.8 GHz. By the standard bandpass to lowpass transformation, a six section filter with the following prototype parameters was found to be necessary$^{(28,30)}$. [Fig. 4.03 - 4, Reference 11]

$g_0 = 1$

$g_1 = .7813$

$g_3 = 1.6896$

$g_4 = 1.535$

$g_5 = 1.4970$

$g_6 = .7098$

$g_7 = 1.1007$

$w_1' = 1$

The stripline realization is shown in Fig. A2.1, each section being resonant at a particular frequency, admittance inversion being accomplished by quarter wavelength coupling. The admittance inverter parameters are related to the lowpass prototype parameters by the following relationship

$$\frac{J_{j,j+1}}{Y_0} \quad j = 1 \text{ to } n-1 \quad = \frac{}{2w_1'} \; \frac{1}{g_{j}, g_{j+1}} \qquad \ldots\ldots(A2.1)$$

$= \text{fractional bandwidth}$

and the even and odd mode impedances(19) of the strip by

$$(Z_{oe})_{j,j+1} \quad j = \text{o to } n = \frac{1}{Y_0}\left[1 + \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right] \qquad \ldots\ldots(A2.2)$$

$$(Z_{oo})_{j,j+1} \quad j = \text{o to } n = \frac{1}{Y_0}\left[1 - \frac{J_{j,j+1}}{Y_0} + \left(\frac{J_{j,j+1}}{Y_0}\right)^2\right] \qquad \ldots\ldots(A2.3)$$

The dimensions of the strip widths $w_{j,j+1}$ (Fig. A2.1) and gaps $S_{j,j+1}$, were then obtained from the computed values of even and odd mode impedances (Fig. 5.05 - 3 (a) and (b) of reference 11). These values are given in Table A2.1.

The dimensions $d_{j,j+1}$ indicated in Table A2.1, are resonator length corrections to account for the fringing capacitance from the end of each strip. The basic length l, indicated in Fig. A 2.1 is a quarter wavelength at the center frequency (2GHz) in the medium of propagation, while the actual strip lengths are shortened by the amount $d_{j,j+1}$.

The completed stripline circuit is shown in Fig. A2.2. Tuning screws (lower photograph of Fig. A2.2)

were inserted at the end of each resonator section, to reduce input mismatch at 2GHz. The frequency characteristics for the uncompensated filter (no tuning screws) are given in Fig. A2.3, indicating a center frequency of 2.1, rather than the theoretical 2GHz. This error would seem to be attributable to overcompensation of fringing capacitance and was corrected by the use of tuning screws at the expense of reduced bandwidth.

j	$w_{j,j+1}$(IN)	$S_{j,j+1}$(IN)	$d_{j,j+1}$(IN)
0	.059	.00525	.0179
1	.0865	.0275	.0206
2	.090	.0395	.0206
3	.0902	.0407	.0206

TABLE A2.1 Stripline Dimensions For Bandpass Filter

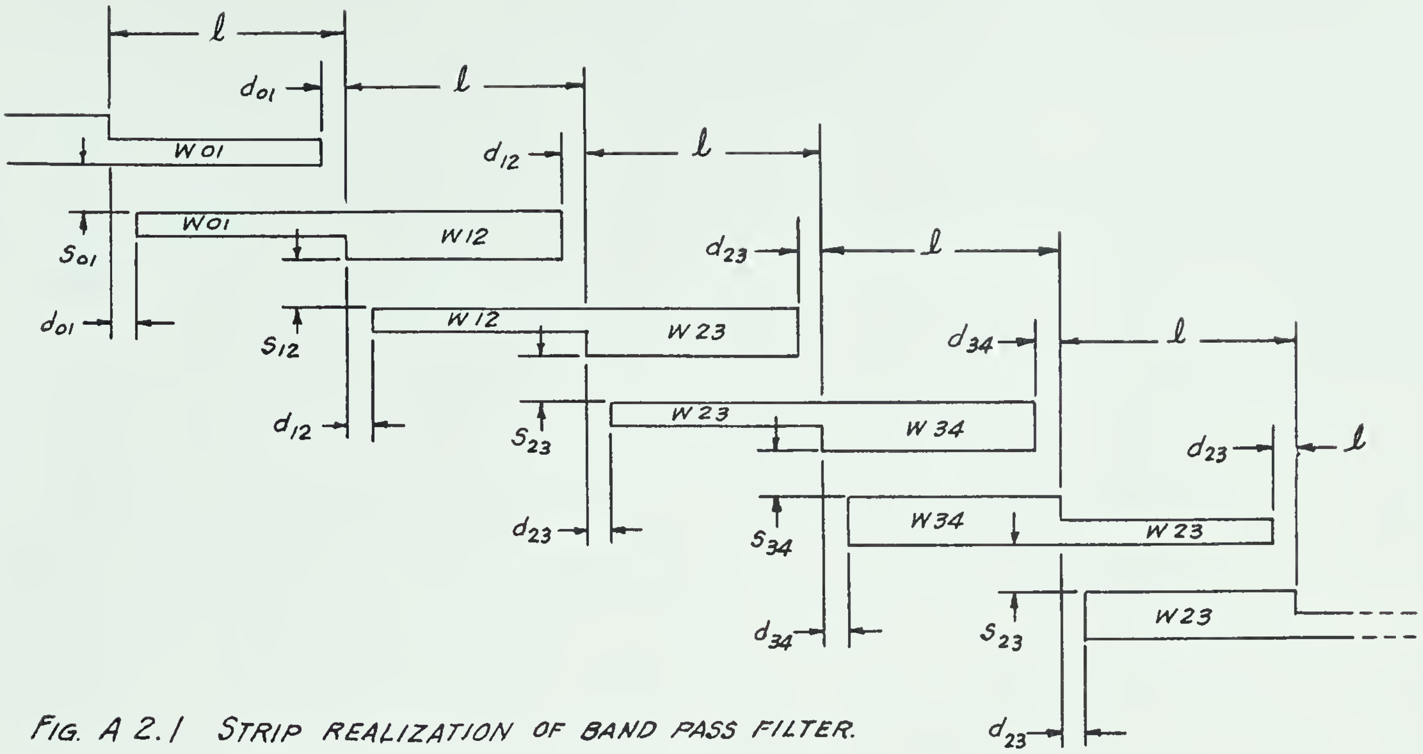


FIG. A 2.1 STRIP REALIZATION OF BAND PASS FILTER.

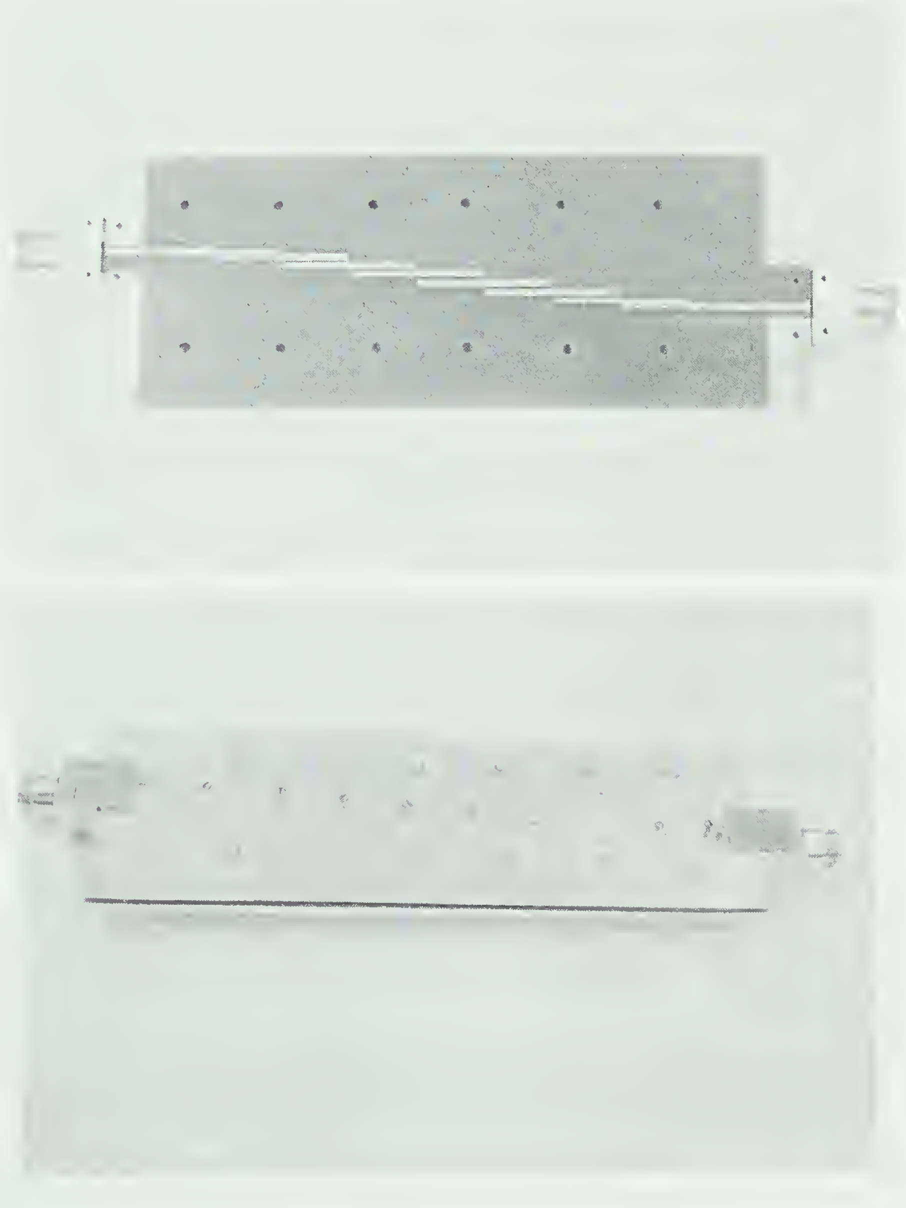


FIG. A 2.2 PHOTOGRAPH OF BAND PASS FILTER.

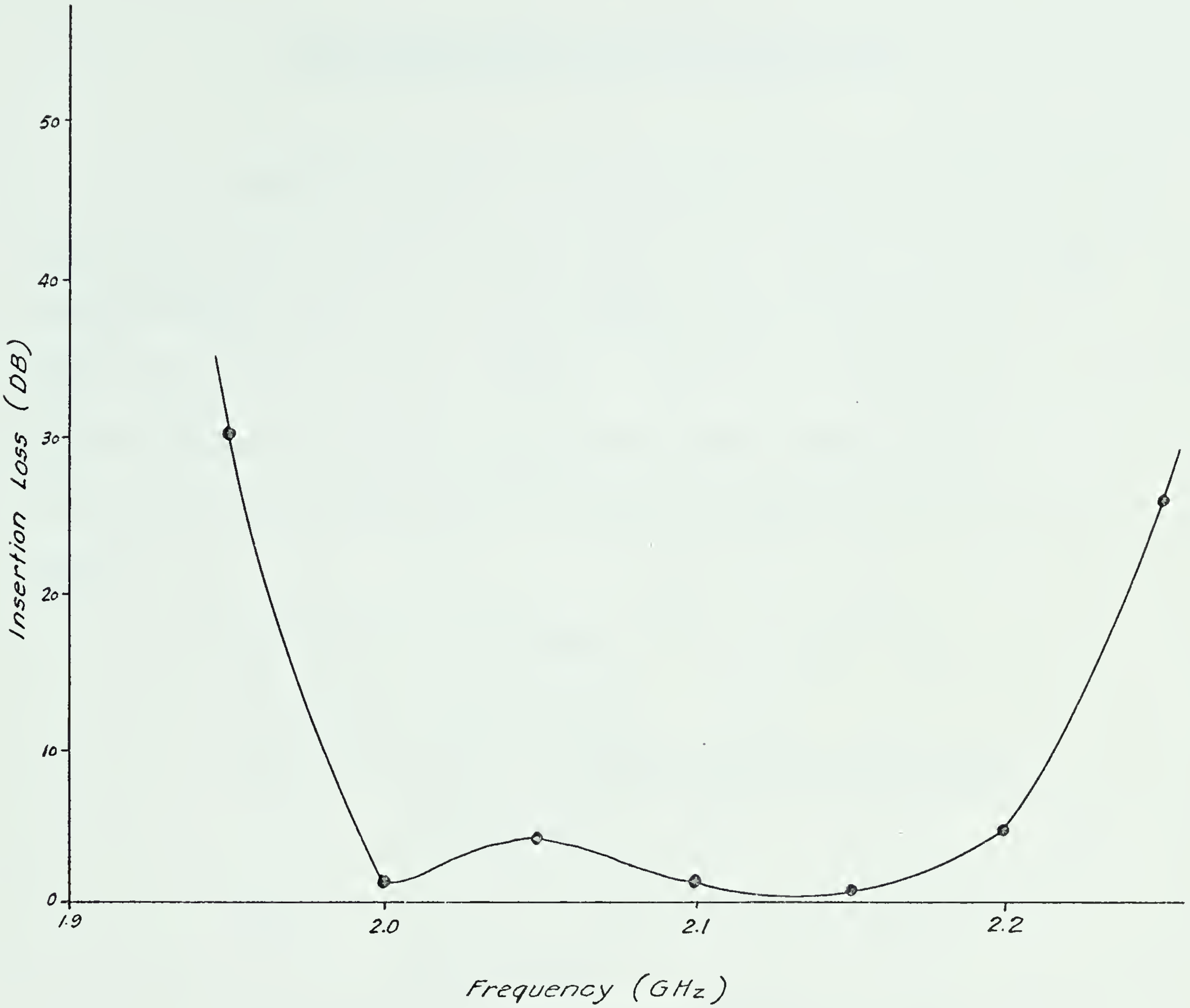


FIG. A2.3 FREQUENCY CHARACTERISTICS OF THE BAND PASS FILTER

APPENDIX III

Matching Utilizing "T" Junction

Input matching for the two diode doubler incorporating the Wilkinson power divider (Section 4.3) was accomplished by means of a compensated coaxial "T" junction (Fig. A3.1). Proper choice of distance x provides for input matching and equal power distribution as illustrated on the Smith chart in Fig. A3.2 where

Z = diode impedance

Y = diode admittance

$Y_{(1)}'$ = diode (1) admittance transformed to junction

$Y_{(2)}'$ = diode (2) admittance transformed to junction

Y_0' = sum of diode admittances at the junction

The effect of individual diode bias variation with respect to total output power is shown in Fig. 4.9. The curve characteristics can be qualitatively predicted by considering the effect of diode impedance variation with bias. Considering diode (1) initially, as bias is decreased from its optimum value: capacitance increases (Fig. 3.9) with an effective impedance decrease(5).

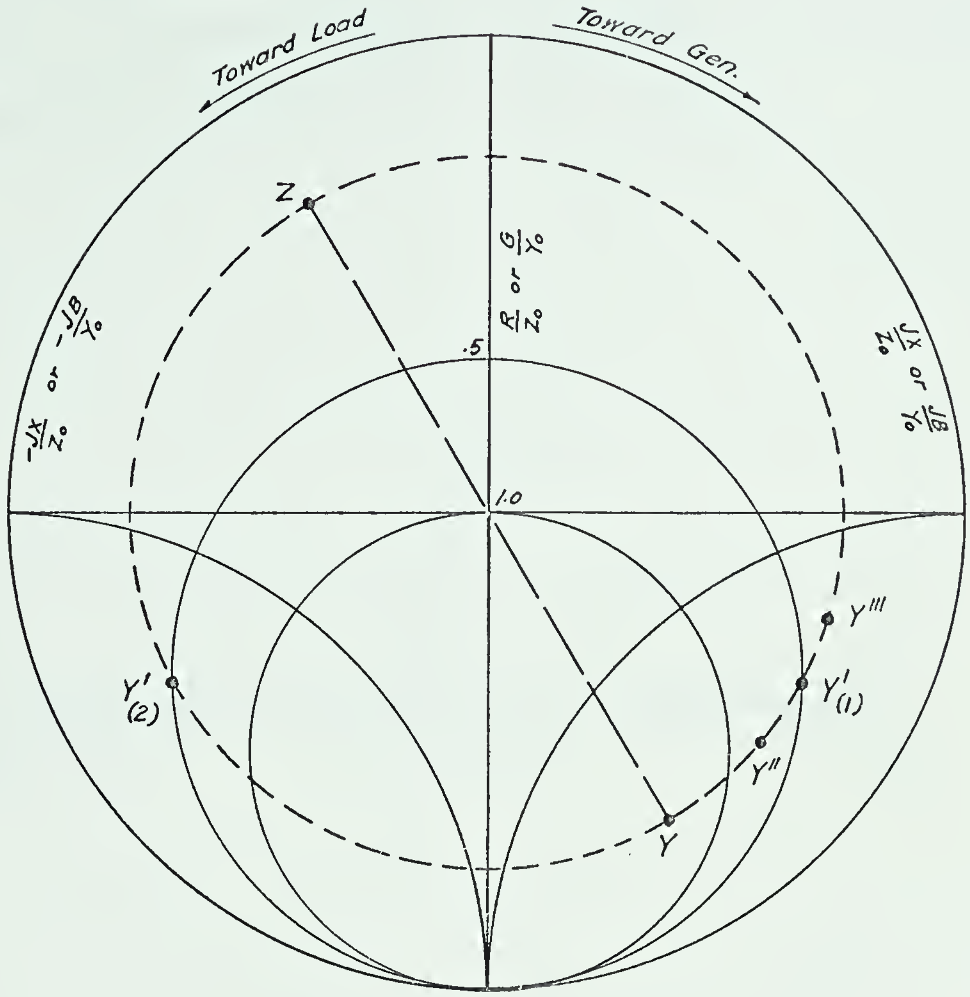

Toward Load
Toward Gen.
Z
$\frac{R}{Z_o}$ or $\frac{G}{Y_o}$
.5
1.0
$-\frac{jX}{Z_o}$ or $-\frac{jB}{Y_o}$
$\frac{jX}{Z_o}$ or $\frac{jB}{Y_o}$
Y' (2)
Y'''
$Y'_{(1)}$
Y''
Y

FIG. A3.2 INPUT MATCHING WITH A "T" JUNCTION.

$Y_{(1)}'$ thus shifts to some new point Y'' on the Smith chart. As $/Y''_{(1)}/ > /Y_{(2)}'/$, more power will be delivered to diode (1), however less input power is available due to a significant mismatch at the junction.

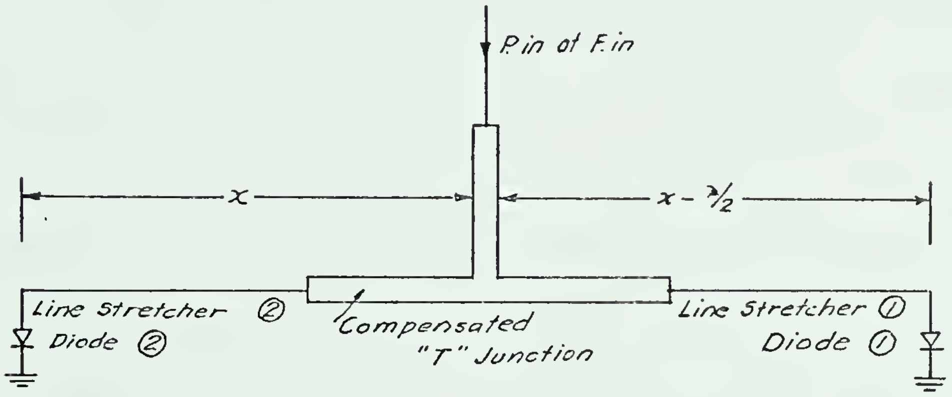


FIG. A3.1 "T" Junction Matching

Thus, decreasing the bias on diode (1) results in less output power available from diodes (1) and (2). Increasing the bias with respect to its optimum value effectively shifts $Y_{(1)}'$ to $Y_{(1)}'''$, resulting in greater power absorption by diode (2) since $/Y_{(1)}'''/ > /Y_{(2)}'/$. The sum of $Y_{(1)}'''$ and $Y_{(2)}'$, the admittance seen by the generator at the junction, is relatively close to the source impedance, resulting in a reasonably

good input match. Thus increasing the bias on diode (1) would result in large amount of available output power from diode (2) and a marked decrease from (1). This qualitative analysis would seem to be born out by experimental results shown in Fig. A3.3. Using a similar argument, curves for bias variation of diode (2) can also be qualitatively explained.

The total output power available is the sum of $P_{10}$and P_{20} (see Figure A3.3). If no additional losses occured total output power versus bias would assume the form shown in Fig. A3.4 for variation of bias of diode (1) and Fig. A3.5 for diode (2). However, since additional losses occur in the Wilkinson summing device for non equiphase, non equiamplitude inputs, some modification will occur.(25) However the experimental results (Fig. 4.9) seem to roughly correspond with the qualitative theory.

By utilizing a Wilkinson device for an input power divider, less sensitivity to variation in bias and thus aging and source frequency shift would occur. However, the problem would be by no means eliminated as mismatch at either output arm in the divider would result in non uniform power distribution and additional losses. A significantly greater amount of circuitry would be needed, as an additional divider and two input matching networks would be required. Although stability

problems and spurious oscillations were not encountered, the Wilkinson device, if used as an input power divider, would provide isolation between input ports, and thus greatly reduce any potential instabilities or higher order resonances.

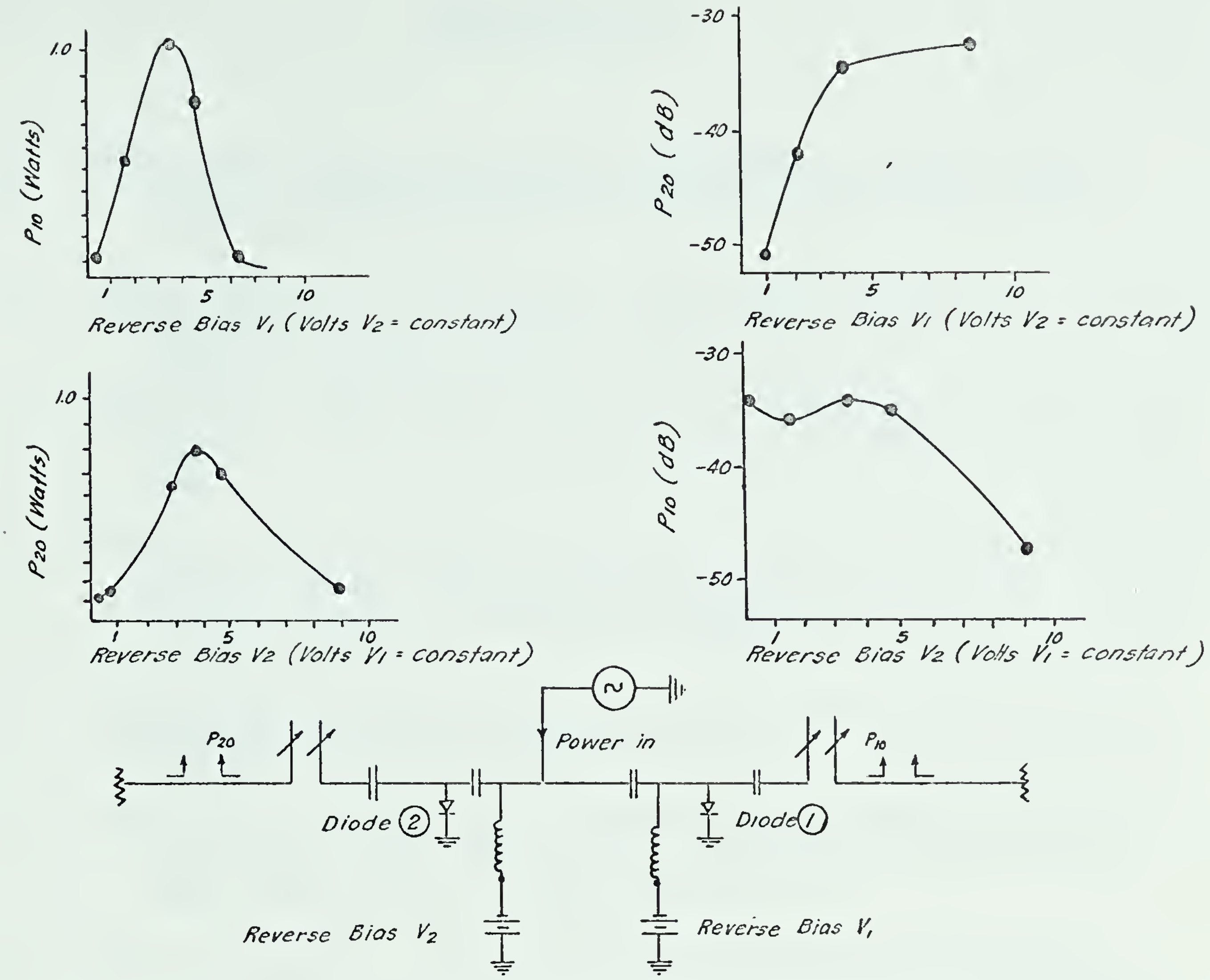


FIG. A 3.3 EFFECT OF BIAS VARIATION ON OUTPUT POWER

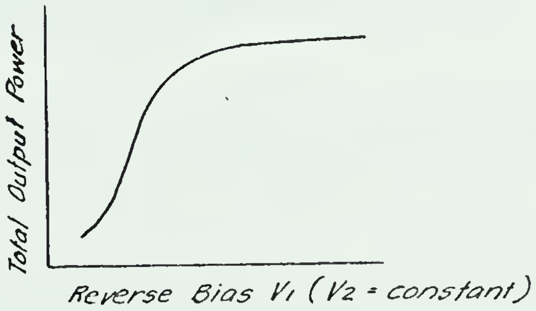


FIG. A 3.4 EFFECT OF BIAS VARIATION OF DIODE ① ON OUTPUT POWER

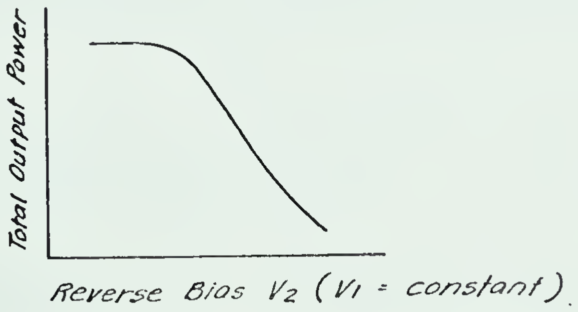


FIG. A 3.5 EFFECT OF BIAS VARIATION OF DIODE ② ON OUTPUT POWER

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